Advance Data Sheet

BROADCOM®

BCM43684

IEEE 802.11ax 4x4 2.4/5 GHz Single-Chip MAC/PHY/Radio

GENERAL DESCRIPTION

The Broadcom® BCM43684 is a dual-band (2.4 GHz and 5 GHz) 4×4 IEEE 802.11ax MAC/PHY/Radio System-on-a-Chip (SoC). The device enables the development of advanced high-efficiency wireless (HE) 802.11ax Access points, repeaters, and WLAN client solutions.

IEEE 802.11ax introduces Orthogonal Frequency-Division Multiple Access (OFDMA) to enhance the multi-user experience. It is an evolutionary step forward from IEEE 802.11ac in that it allows multi-client transmissions in both the uplink and downlink directions. OFDMA multiplexes clients across frequency instead of spatial streams to allow for more concurrent users than MU-MIMO. BSS Coloring allows for better spatial reuse by differentiating Inter-BSS traffic from Intra-BSS traffic, and deferring to Inter-BSS traffic at a higher threshold level. Target Wake Time saves battery life in associated clients, by scheduling Wake Up and Service Periods for STA to be active.

The BCM43684 supports 160 MHz channels and IEEE standardized 1024-QAM modulation. These, combined with a 4x longer OFDM symbol length, allow for a maximum PHY rate of 4.8 Gbps.

IEEE 802.11ax is backward compatible to previous generations and supports MU-MIMO from IEEE 802.11ac.

State-of-the-art security is provided by industry standardized system support for WPA, WPA2 (IEEE 802.11i), and hardware accelerated AES encryption/decryption, coupled with TKIP and IEEE 802.1X support.

Embedded hardware acceleration enables increased system performance and significant reduction in host-CPU utilization in both client and access point (AP) configurations. The BCM43684 also supports the widely accepted and deployed Broadcom Wi-Fi Protected Setup (WPS) for ease-of-use wireless secured networks.

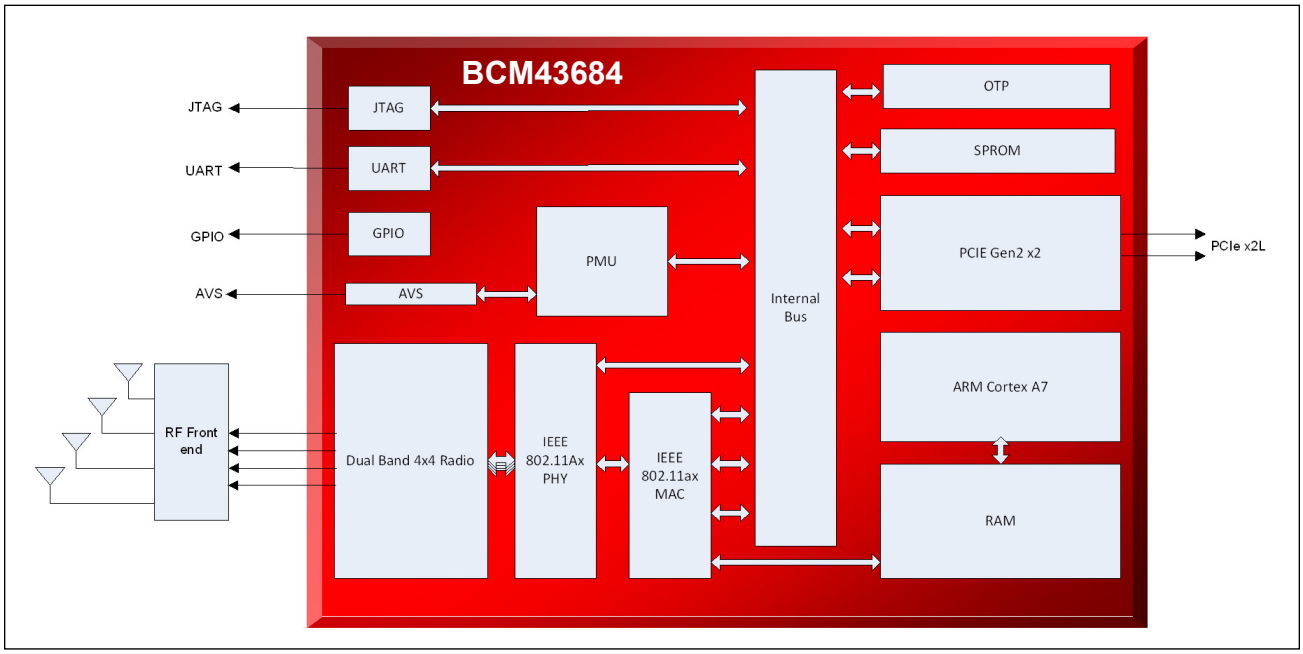
FEATURES

- IEEE 802.11ax compliant.
- Dual-Band OFDMA allows for a higher density of simultaneous users
- Quad-stream spatial multiplexing to 4.8 Gbps data rate.
- IEEE 802.11a/b/g/n/ax, 4×4 160 MHz channels.
- 1024-QAM modulation rates.
- 4×4 MU-MIMO on 80 MHz channels.
- Expanded 5 GHz frequency coverage including spectrum up to 5925 MHz expected to become available under new regulatory rules.
- Supports RangeBoost technology.
- Support for LDPC in both TX and RX for increased wireless coverage.
- 3+1 DSP-based Spectrum Capture and Zero Wait DFS.
- CQI and CSI can be captured and passed to the Host along with the MAC address associated with the captured data.
- Supports Digital Pre-Distortion (DPD) which reduces power consumption and improves Band Edge performance.
- Full IEEE 802.11a/b/g/n/ac legacy compatibility with enhanced performance.
- Complies with PCI Express base specification revision 2.0 for ×2 lane and power management base specification.
- Supports Linux for access point and router applications.
- Comprehensive wireless network security support that includes WPA, WPA2, and AES encryption/decryption.
- Supports full-host CPU IEEE 802.11 packet offload.
- Available in a 13 mm × 13 mm, 284-pin 0.65 mm pitch (FCBGA) package.

APPLICATIONS

- High-performance IEEE 802.11ax access points, routers, and home residential gateways.
- High-performance IEEE 802.11ax enterprise and carrier class access points and business class Integrated Service Routers.

Figure 1: Functional Block Diagram



For a comprehensive list of changes to this document, see the Revision History.

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Section 1: Introduction

General Description

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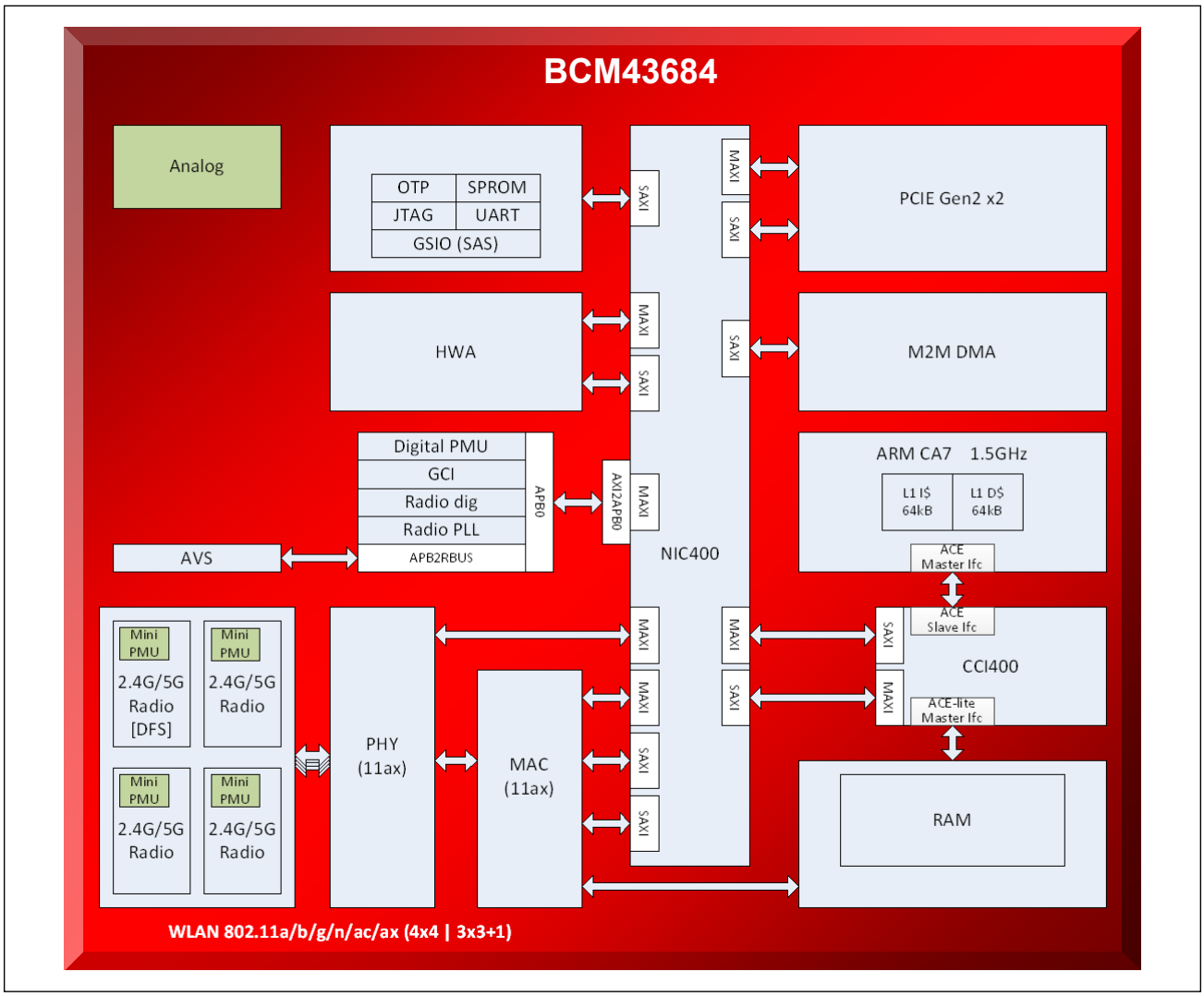
Functional Block Diagram

A functional block diagram of the BCM43684 device is shown below.

Figure 2: Functional Block Diagram



OFDMA (HE) Technology

Orthogonal Frequency-Division Multiple Access (OFDMA) is designed to allow for higher efficiency bi-directional traffic in dense environments. It is an evolutionary step forward from IEEE 802.11ac in that it allows multi-client transmissions in both the uplink and downlink directions. OFDMA multiplexes clients across frequency instead of spatial streams to allow for more concurrent users than MU-MIMO.

To achieve this high efficiency, the IEEE 802.11ax standard places the AP as the central controller of all multi-user operations in both downlink and uplink directions. Through a multitude of information available to the AP, the AP can allocate and divide the spatial domain, frequency domain, and time domain resources among a large number of users in an optimal manner, while reducing medium contention inefficiencies.

The IEEE 802.11ax standard extended the downlink spatial multi-user capabilities of IEEE 802.11ac by allowing the AP to also use OFDMA techniques to multiplex more users simultaneously in the same channel bandwidth. This is achieved by dividing the channel bandwidth into smaller sub-channels called Resource Units (RUs).

On the uplink direction, the AP can also use spatial techniques (UL-MU-MIMO) or OFDMA techniques to allocate resource units to multiple users transmitting traffic simultaneously to the AP. To synchronize user's clocks and frequency references to the AP, the IEEE 802.11ax standard introduced the concept of trigger frames which are used to initiate the simultaneous transmission from each of the users to the AP. The users will use the trigger frame to extract frequency and timing synchronization information, as well as to get detailed commands from the AP in regards to power control information and resource allocations.

Section 2: Functional Description

Global Functions

Power Management

The BCM43684 includes an advanced Power Management Unit (PMU). The PMU provides significant power savings by putting the BCM43684 into various power management states appropriate to the current environment and activities that are being performed. The PMU enables and disables internal regulators, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power-up sequences are fully programmable. Configurable, free-running counters in the PMU are used to turn on/off individual regulators and power. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible. The radio can be put into a low power mode with only one radio chain active to reduce power consumption.

Voltage Regulators

Each radio chain and the crystal and synthesizer blocks contain their own set of integrated Low-Drop Out (LDO) linear regulators that are under PMU control. These regulators require 1.22 V input voltage, which is externally supplied.

AVS Section

AVS is a power-saving technique of the digital 1.0V supply while maintaining performance under various process and operating conditions. The AVS implementation is achieved through the use of a set of on-chip monitors that measure the effects of process, voltage, and temperature on circuit speeds. The monitors are made up of a large set of ring oscillators of different circuit types that represent the different standard cells in the design. The AVS software algorithm drives the external supply to set a voltage such that a minimum speed of the monitors is maintained across process and temperature variations. The steering of the external supply voltage is achieved through the use of an on-chip DAC circuit that controls the feedback voltage of the external regulator. At start-up, the AVS loop is open and the DAC output is tristated. The pre-AVS start-up voltage is determined by the regulator design. This voltage will be sensed by the SoC's ADC circuit and used as the initial voltage when the AVS loop is closed in software.

Reset

At power on, an internal power-on reset circuit provides the necessary reset signal to all internal circuits, including the integrated PHYs. The initialization process loads all pin configurable modes, resets all internal processes, and puts the device into the idle state. During initialization, the clock input source signal must be active and all voltages supplied to the device (3.3V, 1.8V, and 1.22V) must be stable.

When the JTAG_SEL pin is set high, the EXT_POR_L input becomes available on the GPIO_10 pin. This is an optional hard reset input that performs the same function as the internal power-on reset. This allows an external entity to initiate a hard reset of the device. The EXT_POR_L input has an internal pull-up so it does not have to be connected even if it is enabled.

GPIO Interface

There are 16 General-Purpose I/O (GPIO) pins provided on the 13 mm × 13 mm package. These pins can be used to attach to various external devices. Upon power-up and reset, these pins become tristated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. A programmable internal pull-up/pull-down resistor is included on each GPIO. If a GPIO output enable is not asserted, and the corresponding GPIO signal is not being driven externally, the GPIO state is determined by its programmable resistor.

Smart Antenna Subsystem Interface

A two-wire serial interface for controlling a Smart Antenna Subsystem is available. This interface is composed of a clock and data pin, supporting a data rate of up to 16 Mbps. The pins are combined with GPIO_13 and GPIO_14. The data pin carries an antenna index, which is a 16-bit value that is passed through the system from the software driver, on a per-packet basis. The format and contents of the antenna index are defined by the application and antenna management hardware external to the BCM43684. More details can be found in the driver software documentation.

UART Interface

A UART interface is provided in the BCM43684. The UART_RX and UART_TX signals are multiplexed with the GPIO_7 and GPIO_8 signals. This multiplexing can be enabled by software.

OTP

The BCM43684 contains an on-chip One-time Programmable (OTP) area of 16 Kb that can be used for nonvolatile storage of WLAN information such as a MAC address and other hardware-specific parameters.

SPROM Interface

Various hardware configuration parameters may be stored in an external SPROM instead of OTP. The SPROM is read by system software after device reset. In addition, customer-specific parameters may be stored in SPROM, depending on the specific board design.

The 4-wire SPROM interface supports 16-Kbit serial SPROMs by default and also supports 64-Kbit serial SPROMs via a strapping option.

JTAG Interface

The BCM43684 supports the IEEE 1149.1 JTAG boundary-scan standard for testing the device packaging and PCB manufacturing.

SWD Interface

The BCM43684 supports the ARM Serial Wire Debug (SWD) standard to provide software debug access to the ARM A7 processor core. SWD defines two signals: a clock input and a single bidirectional data signal, providing real-time access to system memory without halting the processor or requiring any target resident code. SWD uses an ARM standard bidirectional wire protocol, defined in the ARM Debug Interface v5, to pass data to and from the debugger and the target system in a highly efficient and standard way.

The SWD signals in the BCM43684 can be multiplexed on the JTAG TCK and TMS signals. This is controlled by strapping options.

Crystal Oscillator

The table below lists the requirements for the crystal oscillator.

Table 1: Crystal Oscillator Requirements

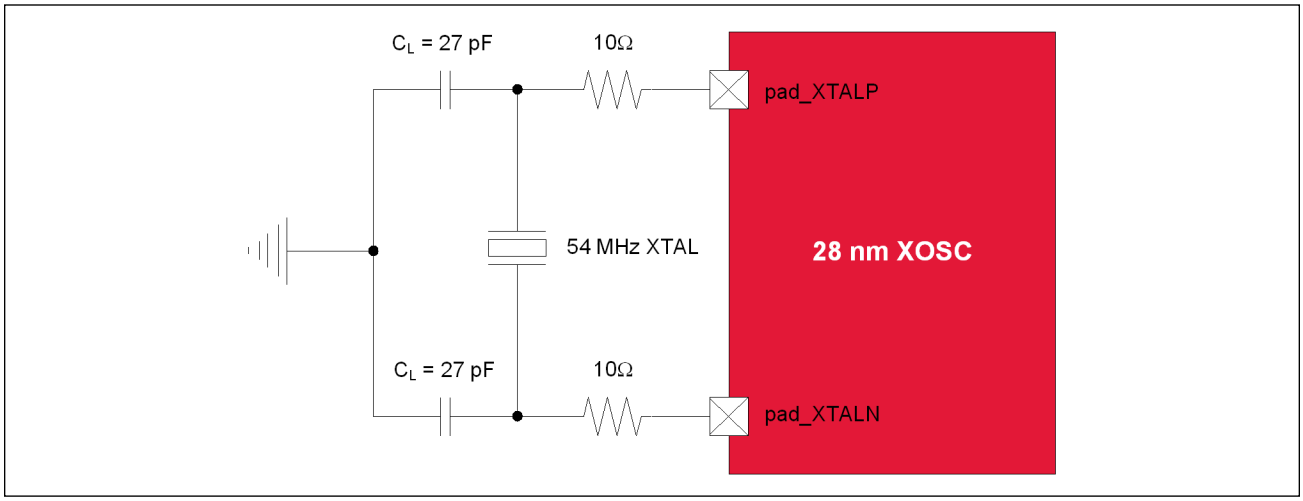
Parameter	*Value*
Frequency	54 MHz
Mode	AT cut, fundamental
Load capacitance	19 pF
ESR	15Ω maximum
Frequency stability	±3 ppm at 25°C
Aging	±1 ppm/year maximum
Drive level	350 µW maximum
Shunt capacitance	5 pF maximum

The following figure shows the recommended oscillator configuration.

Fundamental Crystal Oscillator Mode

This is the minimum-BOM solution, which avoids the necessity of a notch filter. This is the recommended solution for BCM43684.

Figure 3: Suggested Board Components for Fundamental Crystal Operation



The value of the two board capacitors, CL (27 pF), is board layout dependent. This value depends on the stray capacitance between the crystal components and their reference ground plane. This CL (27 pF), plus PCB trace capacitance, plus one chip pin capacitance forms an equivalent of 38 pF on each side of the crystal, which results in 19 pF differentially across the crystal. The 19 pF is the *load capacitance* specified in a typical crystal specification.

A frequency counter can be used to measure the frequency. If the frequency is greater than 54 MHz, the parasitic is smaller than expected so the PCB load cap should be increased; or if the measured frequency is less than 54 MHz, this indicates that the parasitic cap is too high and the load capacitor should be reduced.

The frequency pullability (also known as Trim Sensitivity) of the crystals (ppm shift, pF change in load cap) varies with the crystal type, but is approximately 3 ppm, pF change (meaning a 2 pF change in each of the two capacitors since they are in series). For more information, consult the manufacturer data.

Fundamental Crystal Example

The reference design example uses a crystal from Siward. This crystal is a 54 MHz 4-lead seam package with part number XTL581100-B63-299. The key specifications for this crystal example are the following:

- Body size: 2.5 mm ×2.0 mm, four pins
- Fundamental at 54.000000 MHz
- Load Capacitance: 19 pF
- Tolerance: ±7 ppm maximum, over operating temperature
- Stability: ±10 ppm maximum, over operating temperature
- Aging: ±1 ppm maximum, first year
- ESR: 15Ω maximum, over operating temperature
- Operating Temperature: –30°C to +85°C
- Shunt Capacitance (C0): 5 pF maximum, over operating temperature
- Maximum Drive Level: 200 µW over operating temperature

Host CPU Offload Support

The BCM43684 enables all IEEE 802.11 WLAN processing to be offloaded from the host processor to run on the device equipped with an ARM A7 processor. The device-side IEEE 802.11 software driver components running on the CA7 processor, along with the hardware IEEE 802.11 MAC and microcode, cooperatively perform the WLAN protocol processing function. On the host-side, an IEEE 802.3 Ethernet-like network interface is registered with the native OS network stack and acts as a peer to the device-side IEEE 802.11 driver, communicating via software mailboxes over PCIe.

- Fast CA7 speed at 1.5 GHz.
- Packet chaining (including AMSDU in AMPDU).
- Zero wait state.
- Large memory for ARM: 7 MB RAM.
- Software optimizations based on profiling.
- Backplane frequency @ 240 MHz. Includes I cache (64 KB) and D cache (64 KB).

Power Topology

The BCM43684 requires the following power supplies:

- VDDIO: 1.8V/3.3V
- Radio: 3.3V
- Radio: 1.8V
- Radio: 1.22V
- Digital Core (VDD): 0.95V–1.05V (Changed under control of AVS_Top)

The digital core supply has the option to use either of the following.

1. An external switching regulator with digital control for support of AVS.
2. An internal switching regulator controller, using chip external switching FETs (see Figure 5 on page 16).

Power topology is shown in Figure 4 below.

Figure 4: Power Topology

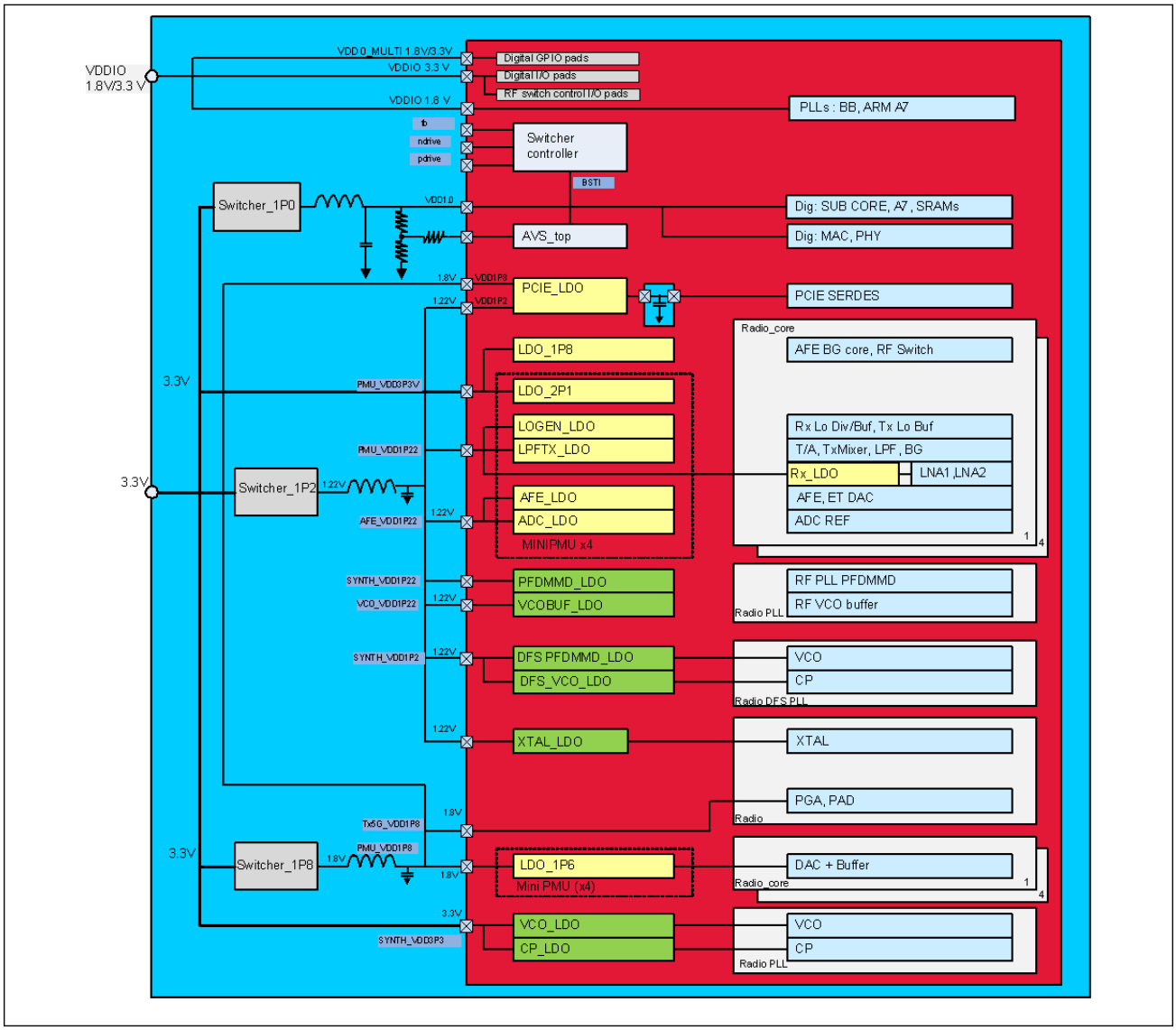
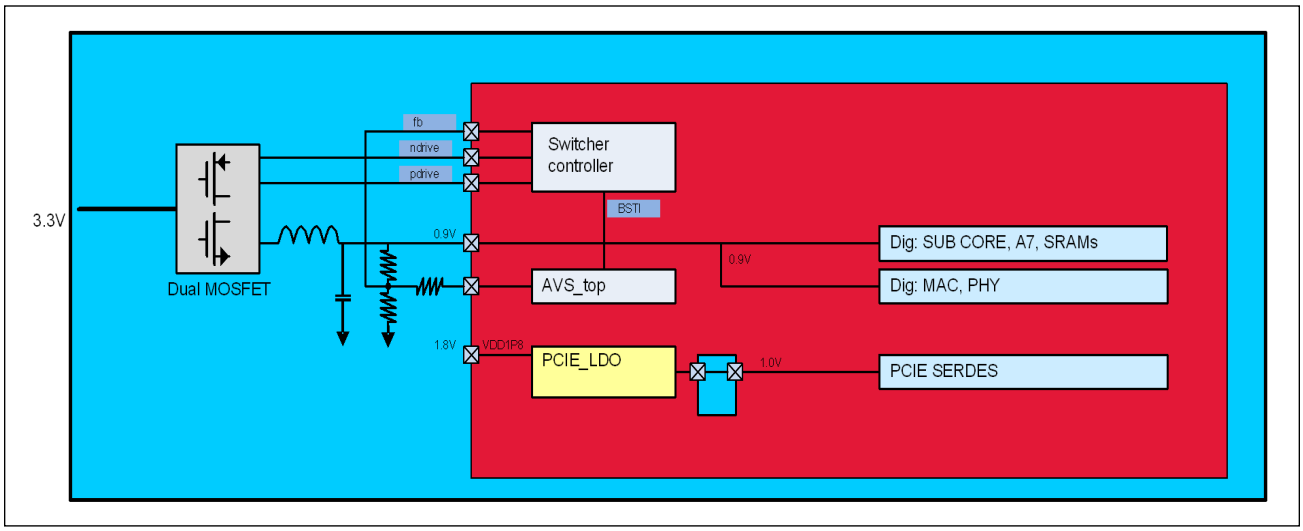


Figure 5: Power Topology with Internal Switching Regulator



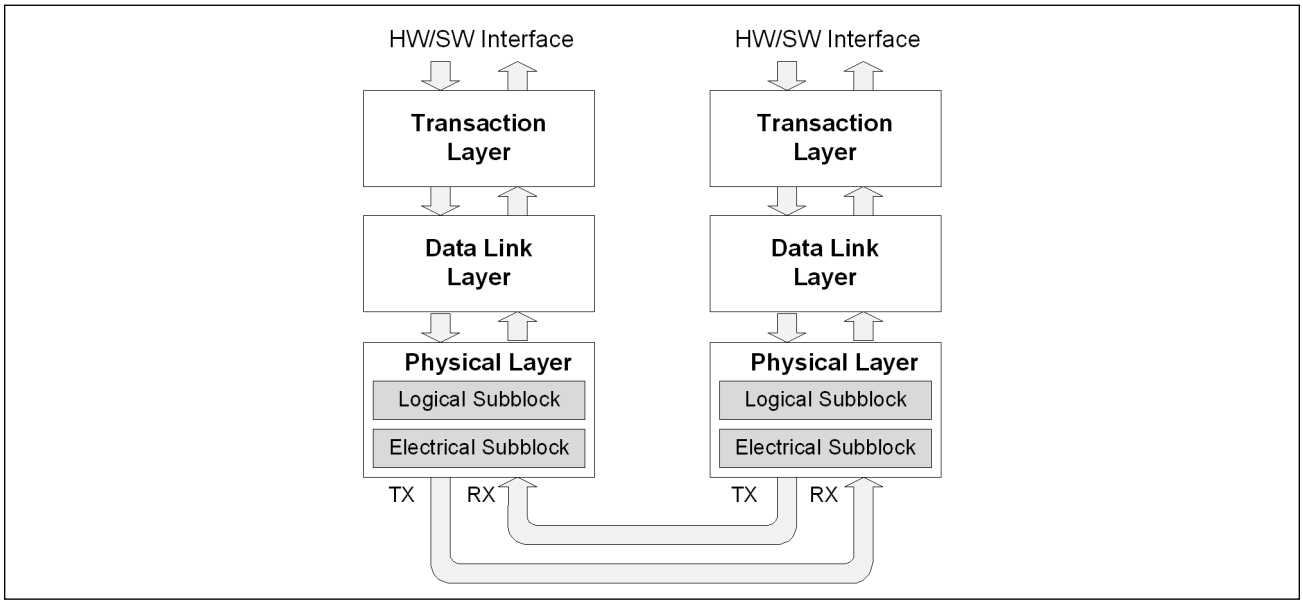
PCI Express Interface

The PCI Express (PCIe) core on the BCM43684 is a high-performance serial I/O interconnect that is protocol-compliant and electrically compatible with the *PCI Express Base Specification v2.0*, supporting a one or two-lane link (x1 or x2). This core contains all the necessary blocks, including logical and electrical functional subblocks to perform PCIe functionality and maintain high-speed links, using existing PCI system configuration software implementations without modification.

Organization of the PCIe core is in logical layers: Transaction Layer, Data Link Layer, and Physical Layer, as shown in the following figure. A configuration or link management block is provided for enumerating the PCIe configuration space and supporting generation and reception of System Management Messages by communicating with PCIe layers.

Each layer is partitioned into dedicated transmit and receive units that allow point-to-point communication between the host and BCM43684 device. The transmit side processes outbound packets while the receive side processes inbound packets. Packets are formed and generated in the Transaction and Data Link Layer for transmission onto the high-speed links and onto the receiving device. A header is added at the beginning to indicate the packet type and any other optional fields.

Figure 6: PCI Express Layer Model



Transaction Layer Interface

The PCIe core employs a packet-based protocol to transfer data between the host and BCM43684 device, delivering new levels of performance and features. The upper layer of the PCIe is the Transaction Layer. The Transaction layer is primarily responsible for assembly and disassembly of Transaction Layer Packets (TLPs). TLP structure contains header, data payload, and End-to-End CRC (ECRC) fields, which are used to communicate transactions, such as read and write requests and other events.

A pipelined full split-transaction protocol is implemented in this layer to maximize efficient communication between devices with credit-based flow control of TLP, which eliminates wasted link bandwidth due to retries.

Data Link Layer

The data link layer serves as an intermediate stage between the transaction layer and the physical layer. Its primary responsibility is to provide reliable, efficient mechanism for the exchange of TLPs between two directly connected components on the link. Services provided by the data link layer include data exchange, initialization, error detection and correction, and retry services.

Data Link Layer Packets (DLLPs) are generated and consumed by the data link layer. DLLPs are the mechanism used to transfer link management information between data link layers of the two directly connected components on the link, including TLP acknowledgment, power management, and flow control.

Physical Layer

The physical layer of the PCIe provides a handshake mechanism between the data link layer and the high-speed signaling used for Link data interchange. This layer is divided into the logical and electrical functional subblocks. Both subblocks have dedicated transmit and receive units that allow for point-to-point communication between the host and BCM43684 device. The transmit section prepares outgoing information passed from the data link layer for transmission, and the receiver section identifies and prepares received information before passing it to the data link layer. This process involves link initialization, configuration, scrambler, and data conversion into a specific format.

Logical Subblock

The logical sub block primary functions are to prepare outgoing data from the data link layer for transmission and identify received data before passing it to the data link layer.

Scrambler/Descrambler

This PCIe PHY component generates pseudo-random sequence for scrambling of data bytes and the idle sequence. On the transmit side, scrambling is applied to characters prior to the 8b/10b encoding. On the receive side, descrambling is applied to characters after 8b/10b decoding. Scrambling may be disabled in polling and recovery for testing and debugging purposes.

8B/10B Encoder/Decoder

The PCIe core on the BCM43684 uses an 8b/10b encoder/decoder scheme to provide DC balancing, synchronizing clock and data recovery, and error detection. The transmission code is specified in the ANSI X3.230-1994, clause 11 and in IEEE 802.3z, 36.2.4.

Using this scheme, 8-bit data characters are treated as 3 bits and 5 bits mapped onto a 4-bit code group and a 6-bit code group, respectively. The control bit in conjunction with the data character is used to identify when to encode one of the twelve Special Symbols included in the 8b/10b transmission code. These code groups are concatenated to form a 10-bit symbol, which is then transmitted serially. Special Symbols are used for link management, frame TLPs, and DLLPs, allowing these packets to be quickly identified and easily distinguished.

Elastic FIFO

An elastic FIFO is implemented in the receiver side to compensate for the differences between the transmit clock domain and the receive clock domain, with worse case clock frequency specified at 600 ppm tolerance. As a result, the transmit and receive clocks can shift one clock every 1666 clocks. In addition, the FIFO adaptively adjusts the elastic level based on the relative frequency difference of the write and read clock. This technique reduces the elastic FIFO size and the average receiver latency by half.

Electrical Subblock

The high-speed signals utilize the Common Mode Logic (CML) signaling interface with on-chip termination and de-emphasis for best-in-class signal integrity. A de-emphasis technique is employed to reduce the effects of Intersymbol Interference (ISI) due to the interconnect by optimizing voltage and timing margins for worst case channel loss. This results in a maximally open “eye” at the detection point, thereby allowing the receiver to receive data with acceptable Bit-Error Rate (BER).

To further minimize ISI, multiple bits of the same polarity that are output in succession are de-emphasized. Subsequent same bits are reduced by a factor of 3.5 dB in power. This amount is specified by PCIe to allow for maximum interoperability while minimizing the complexity of controlling the de-emphasis values. The high-speed interface requires AC coupling on the transmit side to eliminate the DC common mode voltage from the receiver. The range of AC capacitance allowed is 75 nF to 200 nF.

Configuration Space

The PCIe function in the BCM43684 implements the configuration space as defined in the *PCI Express Base Specification v2.0*.

IEEE 802.11ax MAC Description

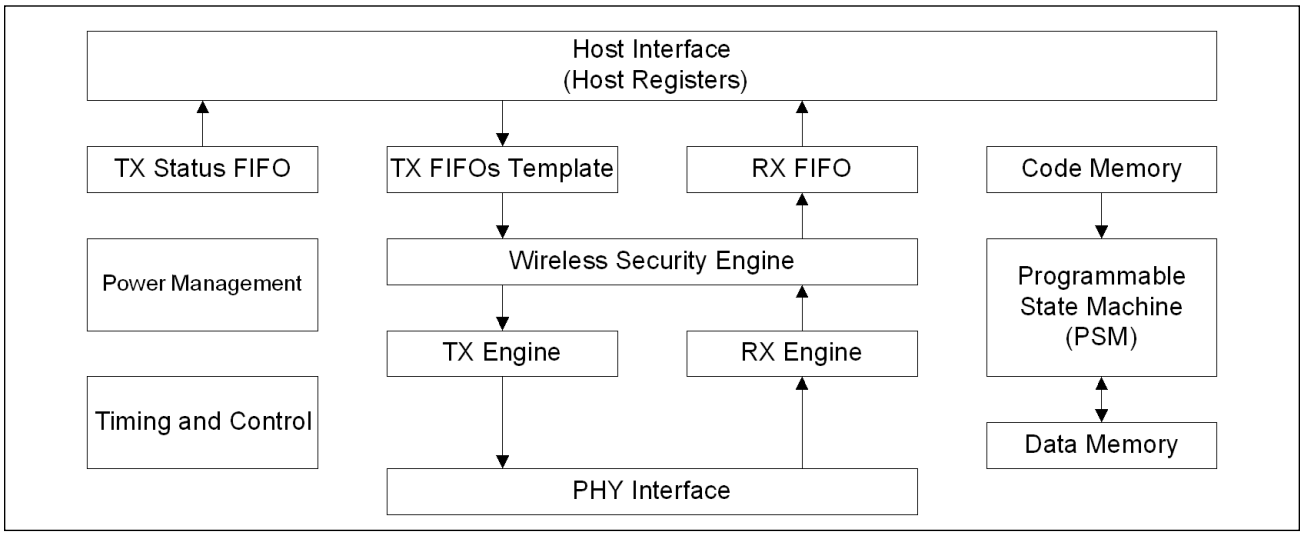
The IEEE 802.11ax MAC features include:

- Enhanced MAC for supporting IEEE 802.11ax features.
- Programmable Access Point (AP) or Station (STA) functionality.
- Programmable Independent Basic Service Set (IBSS) or infrastructure mode.
- Aggregated MPDU (MAC Protocol Data Unit) support for High-throughput (HT).
- Passive scanning.
- Network Allocation Vector (NAV), Interframe Space (IFS), and Timing Synchronization Function (TSF) functionality.
- RTS/CTS procedure.
- Transmission of response frames (ACK/CTS).
- Address filtering of receive frames as specified by IBSS rules.
- Multirate support.
- Programmable Target Beacon Transmission Time (TBTT), beacon transmission/cancellation and programmable Announcement Traffic Indication Message (ATIM) window.
- CF conformance: Setting NAV for neighborhood Point Coordination Function (PCF) operation.
- Security through a variety of encryption schemes including WEP, TKIP, AES, WPA, WAP2, and IEEE 802.1X.
- Power management.
- Statistics counters for MIB support.
- Message Signaled Interrupt (MSI) support.

The MAC core supports the transmission and reception of sequences of packets, together with related timing, without any packet-by-packet driver interaction. Time-critical tasks requiring response times of only a few milliseconds are handled in the MAC core. This achieves the required timing on the medium while keeping the host driver easier to write and maintain. Also, incoming packets are buffered in the MAC core, which allows the MAC driver to process them in bursts, enabling high bandwidth performance.

The MAC driver interacts with the MAC core to prepare queues of packets to transmit and to analyze and forward received packets to upper software layers. The internal blocks of the MAC core are connected to a Programmable State Machine (PSM) through the host interface that connects to the internal bus (see the following figure).

Figure 7: Enhanced MAC Block Diagram



The host interface consists of registers for controlling and monitoring the status of the MAC core and interfacing with the TX/RX FIFOs. For transmit, a total of 1 MB of buffer memory is available that can be dynamically allocated to transmit queues plus template space for beacons, ACKs, and probe responses. Whenever the host has a frame to transmit, the host queues the frame into one of the transmit FIFOs with a TX descriptor containing TX control information. The PSM schedules the transmission on the medium depending on the frame type, transmission rules in IEEE 802.11 protocol, and the current medium occupancy scenario. After the transmission is completed, a TX status is returned to the host, informing the host of the result that got transmitted.

The MAC contains two RX channels that each have dedicated reserved buffer memory. Whenever a frame is received, the frame is sent to the host along with an RX descriptor that contains additional information about the frame reception conditions.

The power management block maintains the information regarding the power management state of the core (and the associated STAs in case of an AP) to help in dynamic decisions by the core regarding frame transmission.

The wireless security engine performs the required encryption/decryption on the TX/RX frames. This block supports separate transmit and receive keys with four shared keys and 50 link-specific keys. The link-specific keys are used to establish a secure link between any two STAs, with the required key being shared between only those two STAs, hence excluding all of the other STAs in the same network from deciphering the communication between those two STAs. The wireless security engine supports the following encryption schemes that can be selected on a per-destination basis:

- None: The wireless security engine acts as a pass-through.
- WEP: 40-bit secure key and 24-bit IV as defined in IEEE Std. 802.11-2007.
- WEP128: 104-bit secure key and 24-bit IV.
- TKIP: IEEE Std. 802.11-2007.
- AES: IEEE Std. 802.11-2007.

The transmit engine is responsible for the byte flow from the TX FIFO to the PHY interface through the encryption engine and the addition of an FCS (CRC-32) as required by IEEE 802.11-2007. Similarly, the

receive engine is responsible for byte flow from the PHY interface to the RX FIFO through the decryption engine and for detection of errors in the RX frame.

The timing block performs the TSF, NAV, and IFS functionality as described in IEEE Std. 802.11-2007.

The Programmable State Machine (PSM) coordinates the operation of different hardware blocks required for both transmission and reception. The PSM also maintains the statistics counters required for MIB support.

IEEE 802.11 PHY Description

The PHY features include:

- Programmable data rates from HT (11n) MCS 0–23 and MCS 32 in 20 MHz and 40 MHz channels, VHT(11ac) MCS 0–9 in 20 MHz, 40 MHz, and 80 MHz channels, and HE (11ax) MCS 0–11 in 20 MHz, 40 MHz, 80 MHz, and 160 MHz channels, providing a maximum 4x4 PHY rate of up to 4803 Mbps.
- Support for all mandatory HE PHY features, including downlink and uplink OFDMA, downlink MU-MIMO, and HE sounding protocol.
- Additional proprietary VHT (11ac) 1024-QAM modulation rates.
- Support for HE guard interval up to 3.2 µs, Short Guard Interval (SGI), and Low-Density Parity Check Coding (LDPC).
- Expanded 5 GHz frequency coverage, including spectrum up to 5925 MHz, is expected to become available under new regulatory rules. If fully sanctioned by the FCC, the new bandwidth will be much less congested, allowing for higher performance and higher network capacity.
- All scrambling, encoding, forward error correction, and modulation in the transmit direction, and inverse operations in the receive direction.
- Advanced digital signal processing technology for best-in-class receive sensitivity.
- Both long and optional short preambles of IEEE 802.11b.
- Resistance to multipath with maximal ratio combining for high throughput and range performance, including improved performance in legacy mode over existing IEEE 802.11a/b/g solutions.
- Automatic Gain Control (AGC).
- Available per-packet channel quality and signal strength measurements.

The PHY core in the BCM43684 provides baseband processing at all mandatory data rates specified in the IEEE 802.11n specification up to 450 Mbps, at all mandatory and optional MCS specified in the IEEE 802.11ac specification up to 2.2 Gbps, and at all mandatory and optional MCS specified in the IEEE 802.11ax standard up to 4.8 Gbps, and the legacy rates specified in IEEE 802.11a/b/g including 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54 Mbps. This core acts as an intermediary between the MAC and the dual-band 2.4 GHz/5 GHz radio, converting back and forth between packets and baseband waveforms.

Dual-Band Radio Transceiver

The world-class Broadcom dual-band radio transceiver is integrated into the BCM43684, which ensures low power consumption and robust communications for applications operating in the 2.4 and 5 GHz bands. Channel bandwidths of 20 MHz, 40 MHz, 80 MHz and 160 MHz are supported as specified in the IEEE 802.11ax standard.

Receiver Path

The BCM43684 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band.

Transmitter Path

Baseband data is modulated and upconverted to the 2.4 GHz ISM band or the 5 GHz U-NII bands, respectively.

Calibration

The BCM43684 features dynamic on-chip calibration, eliminating process variation across components. This enables the device to be used in high-volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation.

Section 3: BGA Ball Assignments

Ballout Diagram

Figure 8: Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A		RF5G_OUT_C0	VSSC_ANALOG	VSSC_ANALOG	FEMCTRL_3	FEMCTRL_4	FEMCTRL_11	FEMCTRL_12	TRACE_0			TRACE_8	PCIE_AVSS	PCIE_AVSS	TDP1	PCIE_AVSS	RDN1	RDP1	PCIE_AVSS	A
B	RF5G_IN_C0	VSSC_ANALOG		VSSC_ANALOG	FEMCTRL_0	FEMCTRL_5	FEMCTRL_10	FEMCTRL_13	TRACE_2	VSS	VSS	TRACE_7	PCIE_AVSS	PCIE_AVSS	TDN1	PCIE_AVSS	PCIE_AVSS	PCIE_AVSS	PCIE_AVSS	B
C	RF2G_IN_C0	VSSC_ANALOG	WIFI_TX_VDD1_V1P8	TSSI_C0					TRACE_3			TRACE_9	PCIE_AVSS	PCIE_VD D_1P8	PCIE_AVSS					C
D		RF2G_OUT_C0	VSSC_ANALOG	TSSI_C1	FEMCTRL_1	FEMCTRL_6	FEMCTRL_9	FEMCTRL_14	TRACE_4	VSS	VSS	TRACE_12	TESTP	PCIE_LDO_OUT_1P0	PCIE_AVSS	PCIE_AVSS	TDN0	RDN0	RDP0	D
E			WIFI_MIX_VDD1_V1P8	VSSC_ANALOG	FEMCTRL_2	FEMCTRL_7	FEMCTRL_8	FEMCTRL_15	TRACE_5			TRACE_13	TESTN	PCIE_LDO_SENSE	PCIE_AVSS	TVDD1P0	TDP0			E
F		RF5G_OUT_C1	WIFI_PMU_VDD_V1P2V_0	VSSC_ANALOG					TRACECTL	VSS	VSS	TRACE_11	PCIE_AVSS	PCIE_LDO_IN_1P2		PVDD1P0	RVDD1P0	REFCLKP	REFCLKN	F
G	RF5G_IN_C1	VSSC_ANALOG		WIFI_PMU_VDD_V1P2_1	VSS	VDDO_V3P3	VDDO_V1P8	VDDO_V1P8	TRACECLK			TRACE_15	PCIE_AVSS				VSS	VSS	VSS	G
H	RF2G_IN_C1	VSSC_ANALOG	VSSC_ANALOG	VSSC_ANALOG	VSS	VDD	VDD	VDD	TRACE_1	TRACE_6	TRACE_10	TRACE_14			VSS	VDD	VDD	VDD	VDD	H
J		RF2G_OUT_C1		VSSC_ANALOG	VSS	VSS	VDD	VDD	VSS	VSS	VSS	VDD	VDD	VDD	VSS	VSS	VDD	VDD	VSS	J
K				VSSC_ANALOG	VDD	VDD	VSS	VSS	VDD	VDD	VSS	VSS	VSS	VSS	VDD	VDD	VSS	VSS	VDD	K
L		RF5G_OUT_C2	RADIO_TEST_1	RADIO_TEST_4	VDD	VDD	VSS	VSS	VDD	VDD	VDD	BBPLL_PAD_VDD1P8	VSS	VSS	VDD	VDD	VSS	VSS	VDD	L
M	RF5G_IN_C2	VSSC_ANALOG	RADIO_TEST_2	RADIO_TEST_3	VSS	VSS	VDD	VDD	VSS	VSS	VDD	BBPLL_PAD_VSS	VDD	VDD	VSS	VSS	VDD	VDD	VSS	M
N	RF2G_IN_C2	VSSC_ANALOG		VSSC_ANALOG	VSS				VSS	VDDO_V1P8	VDDO_V1P8		VDD	VSS		CPUPLL_PAD_VDD1P8	VDD	VDD	PVSS_SW	N
P		RF2G_OUT_C2		VSSC_ANALOG	WIFI_PMU_VDD_V3P3	SYNTH_VDD_V1P22V_SYNTH0	VCOBUF_VDD_V1P22V_SYNTH0		MULTI_VDDO_SET_3P3	VDDO_MULTI	VDDO_V3P3		VDD	VDD		CPUPLL_PAD_VSS	VSS	VSS	PVDDIN_SW	P
R			WIFI_PMU_VDD_V1P2_2	TSSI_C2	VCOBUF_VDD_V1P22V_SYNTH1		SYNTH_VDD_V3P3V_SYNTH0	GPIO_9	GPIO_10	GPIO_7	GPIO_2		SPROM_DOUT	SPROM_CLK	SPROM_CS				NDRIVE_SW	R
T		RF5G_OUT_C3	TSSI_C3	WIFI_PMU_VDD_V1P8		XTAL_GND	XTAL_GND	GPIO_12	GPIO_11	GPIO_8	GPIO_3	RF_DISABLE_L	BSC_SCL	JTAG_SEL	SPROM_DIN	STB_PVTMON_ADC	STB_PVTMON_DAC	VSS_SW	PDRIVE_SW	T
U	RF5G_IN_C3	VSSC_ANALOG	WIFI_TX_VDD0_V1P8	SYNTH_VDD_V1P22V_SYNTH1			WRF_XTAL_VDD_V1P8	GPIO_13		GPIO_6	VSS	BSC_SDA		SWREG_DIS		AVSS_AVS		VSS	SENSE_SW	U
V	RF2G_IN_C3	VSSC_ANALOG	WIFI_MIX_VDD0_V1P8	SYNTH_VDD_V3P3V_SYNTH1	XTAL_GND	XTAL_GND		GPIO_14	VSS	GPIO_5		GPIO_1	VSS	PCIE_CLKREQ_L		AVDD_1P8		VDD	VDD_DIG_SENSE_SW	V
W		RF2G_OUT_C3	VSSC_ANALOG	XTAL_GND	XTAL_N	XTAL_P	XTAL_GND	GPIO_15		GPIO_4	VSS	GPIO_0		PERST_L		PCI_PME_L		AVDDIN_SW		W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Ball and Signal Definitions

Signals by Ball Number

Table 2: Signals by Ball Number

Ball	Signal Name
A2	RF5G_OUT_C0
A3	GND
A4	GND
A5	FEMCTRL_3
A6	FEMCTRL_4
A7	FEMCTRL_11
A8	FEMCTRL_12
A9	TRACE_0
A12	TRACE_8
A13	GND
A14	GND
A15	TDP1
A16	GND
A17	RDN1
A18	RDP1
A19	GND
B1	RF5G_IN_C0
B2	GND
B4	GND
B5	FEMCTRL_0
B6	FEMCTRL_5
B7	FEMCTRL_10
B8	FEMCTRL_13
B9	TRACE_2
B10	GND
B11	GND
B12	TRACE_7
B13	GND
B14	GND
B15	TDN1
B16	GND
B17	GND
B18	GND
B19	GND

Ball	Signal Name
C1	RF2G_IN_C0
C2	GND
C3	WIFI_TX_VDD1_V1P8
C4	TSSI_C0
C9	TRACE_3
C12	TRACE_9
C13	GND
C14	PCIE_VDD_1P8
C15	GND
D2	RF2G_OUT_C0
D3	GND
D4	TSSI_C1
D5	FEMCTRL_1
D6	FEMCTRL_6
D7	FEMCTRL_9
D8	FEMCTRL_14
D9	TRACE_4
D10	GND
D11	GND
D12	TRACE_12
D13	TESTP
D14	PCIE_LDO_OUT_1P0
D15	GND
D16	GND
D17	TDN0
D18	RDN0
D19	RDP0
E3	WIFI_MIX_VDD1_V1P8
E4	GND
E5	FEMCTRL_2
E6	FEMCTRL_7
E7	FEMCTRL_8
E8	FEMCTRL_15
E9	TRACE_5

Ball	Signal Name
E12	TRACE_13
E13	TESTN
E14	PCIE_LDO_SENSE
E15	GND
E16	TVDD1P0
E17	TDP0
F2	RF5G_OUT_C1
F3	WIFI_PMU_VDD_V1P2V_0
F4	GND
F9	TRACECTL
F10	GND
F11	GND
F12	TRACE_11
F13	GND
F14	PCIE_LDO_IN_1P2
F16	PVDD1P0
F17	RVDD1P0
F18	REFCLKP
F19	REFCLKN
G1	RF5G_IN_C1
G2	GND
G4	WIFI_PMU_VDD_V1P2_1
G5	GND
G6	VDDO_V3P3
G7	VDDO_V1P8
G8	VDDO_V1P8
G9	TRACECLK
G12	TRACE_15
G13	GND
G17	GND
G18	GND
G19	GND
H1	RF2G_IN_C1
H2	GND
H3	GND
H4	GND
H5	GND
H6	VDD
H7	VDD
H8	VDD
H9	TRACE_1
H10	TRACE_6
H11	TRACE_10
H12	TRACE_14
H15	GND
H16	VDD
H17	VDD
H18	VDD
H19	VDD
J2	RF2G_OUT_C1
J4	GND
J5	GND
J6	GND
J7	VDD
J8	VDD
J9	GND
J10	GND
J11	GND
J12	VDD
J13	VDD
J14	VDD
J15	GND
J16	GND
J17	VDD
J18	VDD
J19	GND
K4	GND
K5	VDD
K6	VDD
K7	GND
K8	GND
K9	VDD
K10	VDD
K11	GND
K12	GND
K13	GND
K14	GND
K15	VDD
K16	VDD
K17	GND

Ball	Signal Name
K18	GND
K19	VDD
L2	RF5G_OUT_C2
L3	RADIO_TEST_1
L4	RADIO_TEST_4
L5	VDD
L6	VDD
L7	GND
L8	GND
L9	VDD
L10	VDD
L11	VDD
L12	BBPLL_PAD_VDD1P8
L13	GND
L14	GND
L15	VDD
L16	VDD
L17	GND
L18	GND
L19	VDD
M1	RF5G_IN_C2
M2	GND
M3	RADIO_TEST_2
M4	RADIO_TEST_3
M5	GND
M6	GND
M7	VDD
M8	VDD
M9	GND
M10	GND
M11	VDD
M12	GND
M13	VDD
M14	VDD
M15	GND
M16	GND
M17	VDD
M18	VDD
M19	GND
N1	RF2G_IN_C2

Ball	Signal Name
N2	GND
N4	GND
N5	GND
N9	GND
N10	VDDO_V1P8
N11	VDDO_V1P8
N13	VDD
N14	GND
N16	CPUPLL_PAD_VDD1P8
N17	VDD
N18	VDD
N19	GND
P2	RF2G_OUT_C2
P4	GND
P5	WIFI_PMU_VDD_V3P3
P6	SYNTH_VDD_V1P22V_SYNTH0
P7	VCOBUF_VDD_V1P22V_SYNTH0
P9	MULTI_VDDO_SET_3P3
P10	VDDO_MULTI
P11	VDDO_V3P3
P13	VDD
P14	VDD
P16	GND
P17	GND
P18	GND
P19	PVDDIN_SW
R3	WIFI_PMU_VDD_V1P2_2
R4	TSSI_C2
R5	VCOBUF_VDD_V1P22V_SYNTH1
R7	SYNTH_VDD_V3P3V_SYNTH0
R8	GPIO_9
R9	GPIO_10
R10	GPIO_7
R11	GPIO_2
R13	SPROM_DOUT
R14	SPROM_CLK
R15	SPROM_CS
R19	NDRIVE_SW
T2	RF5G_OUT_C3
T3	TSSI_C3

Ball	Signal Name
T4	WIFI_PMU_VDD_V1P8
T6	XTAL_GND
T7	XTAL_GND
T8	GPIO_12
T9	GPIO_11
T10	GPIO_8
T11	GPIO_3
T12	RF_DISABLE_L
T13	BSC_SCL
T14	JTAG_SEL
T15	SPROM_DIN
T16	STB_PVTMON_ADC
T17	STB_PVTMON_DAC
T18	GND
T19	PDRIVE_SW
U1	RF5G_IN_C3
U2	GND
U3	WIFI_TX_VDD0_V1P8
U4	SYNTH_VDD_V1P22V_SYNTH1
U7	WRF_XTAL_VDD_V1P8
U8	GPIO_13
U10	GPIO_6
U11	GND
U12	BSC_SDA
U14	SWREG_DIS
U16	GND
U18	GND
U19	SENSE_SW
V1	RF2G_IN_C3
V2	GND
V3	WIFI_MIX_VDD0_V1P8
V4	SYNTH_VDD_V3P3V_SYNTH1
V5	XTAL_GND
V6	XTAL_GND
V8	GPIO_14
V9	GND
V10	GPIO_5
V12	GPIO_1
V13	GND
V14	PCIE_CLKREQ_L
V16	AVDD_1P8
V18	VDD
V19	VDD_DIG_SENSE_SW
W2	RF2G_OUT_C3
W3	GND
W4	XTAL_GND
W5	XTAL_N
W6	XTAL_P
W7	XTAL_GND
W8	GPIO_15
W10	GPIO_4
W11	GND
W12	GPIO_0
W14	PERST_L
W16	PCI_PME_L
W18	AVDDIN_SW

Signals by Signal Name

Table 3: Signals by Signal Names

Signal Name	Ball
AVDD_1P8	V16
AVDDIN_SW	W18
BBPLL_PAD_VDD1P8	L12
BSC_SCL	T13
BSC_SDA	U12
CPUPLL_PAD_VDD1P8	N16
FEMCTRL_0	B5
FEMCTRL_1	D5
FEMCTRL_10	B7
FEMCTRL_11	A7
FEMCTRL_12	A8
FEMCTRL_13	B8
FEMCTRL_14	D8
FEMCTRL_15	E8
FEMCTRL_2	E5
FEMCTRL_3	A5
FEMCTRL_4	A6
FEMCTRL_5	B6
FEMCTRL_6	D6
FEMCTRL_7	E6
FEMCTRL_8	E7
FEMCTRL_9	D7
GND	A13
GND	A14
GND	A16
GND	A19
GND	A3
GND	A4
GND	B10
GND	B11
GND	B13
GND	B14
GND	B16
GND	B17
GND	B18
GND	B19
GND	B2
GND	B4
GND	C13
GND	C15
GND	C2
GND	D10
GND	D11
GND	D15
GND	D16
GND	D3
GND	E15
GND	E4
GND	F10
GND	F11
GND	F13
GND	F4
GND	G13
GND	G17
GND	G18
GND	G19
GND	G2
GND	G5
GND	H15
GND	H2
GND	H3
GND	H4
GND	H5
GND	J10
GND	J11
GND	J15
GND	J16
GND	J19
GND	J4
GND	J5
GND	J6
GND	J9
GND	K11
GND	K12
GND	K13

Signal Name	Ball
GND	K14
GND	K17
GND	K18
GND	K4
GND	K7
GND	K8
GND	L13
GND	L14
GND	L17
GND	L18
GND	L7
GND	L8
GND	M10
GND	M12
GND	M15
GND	M16
GND	M19
GND	M2
GND	M5
GND	M6
GND	M9
GND	N14
GND	N19
GND	N2
GND	N4
GND	N5
GND	N9
GND	P16
GND	P17
GND	P18
GND	P4
GND	T18
GND	U11
GND	U16
GND	U18
GND	U2
GND	V13
GND	V2
GND	V9
GND	W11

Signal Name	Ball
GND	W3
GPIO_0	W12
GPIO_1	V12
GPIO_10	R9
GPIO_11	T9
GPIO_12	T8
GPIO_13	U8
GPIO_14	V8
GPIO_15	W8
GPIO_2	R11
GPIO_3	T11
GPIO_4	W10
GPIO_5	V10
GPIO_6	U10
GPIO_7	R10
GPIO_8	T10
GPIO_9	R8
JTAG_SEL	T14
NDRIVE_SW	R19
PCI_PME_L	W16
PCIE_CLKREQ_L	V14
PCIE_LDO_IN_1P2	F14
PCIE_LDO_OUT_1P0	D14
PCIE_LDO_SENSE	E14
PCIE_VDD_1P8	C14
PDRIVE_SW	T19
PERST_L	W14
PVDD1P0	F16
PVDDIN_SW	P19
RADIO_TEST_1	L3
RADIO_TEST_2	M3
RADIO_TEST_3	M4
RADIO_TEST_4	L4
RDN0	D18
RDN1	A17
RDP0	D19
RDP1	A18
REFCLKN	F19
REFCLKP	F18
RF_DISABLE_L	T12

Signal Name	Ball
RF2G_IN_C0	C1
RF2G_IN_C1	H1
RF2G_IN_C2	N1
RF2G_IN_C3	V1
RF2G_OUT_C0	D2
RF2G_OUT_C1	J2
RF2G_OUT_C2	P2
RF2G_OUT_C3	W2
RF5G_IN_C0	B1
RF5G_IN_C1	G1
RF5G_IN_C2	M1
RF5G_IN_C3	U1
RF5G_OUT_C0	A2
RF5G_OUT_C1	F2
RF5G_OUT_C2	L2
RF5G_OUT_C3	T2
RVDD1P0	F17
SENSE_SW	U19
SPROM_CLK	R14
SPROM_CS	R15
SPROM_DIN	T15
SPROM_DOUT	R13
STB_PVTMON_ADC	T16
STB_PVTMON_DAC	T17
SWREG_DIS	U14
SYNTH_VDD_V1P22V_SYNTH0	P6
SYNTH_VDD_V1P22V_SYNTH1	U4
SYNTH_VDD_V3P3V_SYNTH0	R7
SYNTH_VDD_V3P3V_SYNTH1	V4
TDN0	D17
TDN1	B15
TDP0	E17
TDP1	A15
TESTN	E13
TESTP	D13
TRACE_0	A9
TRACE_1	H9
TRACE_10	H11
TRACE_11	F12
TRACE_12	D12
TRACE_13	E12
TRACE_14	H12
TRACE_15	G12
TRACE_2	B9
TRACE_3	C9
TRACE_4	D9
TRACE_5	E9
TRACE_6	H10
TRACE_7	B12
TRACE_8	A12
TRACE_9	C12
TRACECLK	G9
TRACECTL	F9
TSSI_C0	C4
TSSI_C1	D4
TSSI_C2	R4
TSSI_C3	T3
TVDD1P0	E16
VCOBUF_VDD_V1P22V_SYNTH0	P7
VCOBUF_VDD_V1P22V_SYNTH1	R5
VDD	H16
VDD	H17
VDD	H18
VDD	H19
VDD	H6
VDD	H7
VDD	H8
VDD	J12
VDD	J13
VDD	J14
VDD	J17
VDD	J18
VDD	J7
VDD	J8
VDD	K10
VDD	K15
VDD	K16
VDD	K19
VDD	K5
VDD	K6

Signal Name	Ball
VDD	K9
VDD	L10
VDD	L11
VDD	L15
VDD	L16
VDD	L19
VDD	L5
VDD	L6
VDD	L9
VDD	M11
VDD	M13
VDD	M14
VDD	M17
VDD	M18
VDD	M7
VDD	M8
VDD	N13
VDD	N17
VDD	N18
VDD	P13
VDD	P14
VDD	V18
VDD_DIG_SENSE_SW	V19
MULTI_VDDO_SET_3P3	P9
VDDO_V1P8	G7
VDDO_V1P8	G8
VDDO_V1P8	N10
VDDO_V1P8	N11
VDDO_V3P3	G6
VDDO_MULTI	P10
VDDO_V3P3	P11
WIFI_MIX_VDD0_V1P8	V3
WIFI_MIX_VDD1_V1P8	E3
WIFI_PMU_VDD_V1P2_1	G4
WIFI_PMU_VDD_V1P2_2	R3
WIFI_PMU_VDD_V1P2V_0	F3
WIFI_PMU_VDD_V1P8	T4
WIFI_PMU_VDD_V3P3	P5
WIFI_TX_VDD0_V1P8	U3
WIFI_TX_VDD1_V1P8	C3

Signal Name	Ball
WRF_XTAL_VDD_V1P8	U7
XTAL_GND	T6
XTAL_GND	T7
XTAL_GND	V5
XTAL_GND	V6
XTAL_GND	W4
XTAL_GND	W7
XTAL_N	W5
XTAL_P	W6

Section 4: Signal and Pin Descriptions

Package Signal Descriptions

The signal name, type, and description of each pin in the BCM43684 packages are listed in the following table. The symbols shown under Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any. See also Table 5 on page 40 for resistor strapping options.

Table 4: Signal Descriptions

Signal	*284-pin ERFCBGA*	*Type*	*Description*
Crystal Oscillator			
XTAL_P	W6	I	P input of 54 MHz on-chip XTAL oscillator differential input
XTAL_N	W5	I	N input of 54 MHz on-chip XTAL oscillator differential input
SPROM Interface			
SPROM_CLK	R14	O	SPROM clock output (3.3V i/f)
SPROM_CS	R15	O	SPROM chip select (3.3V i/f)
SPROM_DIN	T15	I	SPROM data in (3.3V i/f)
SPROM_DOUT	R13	I	SPROM data out (3.3V i/f)
PCI Express Interface			
PCIE_CLKREQ_L	V14	OD	PCIe clock request signal indicates that the refclk to the PCIe interface can be gated (3.3V i/f) 1 = The clock can be gated. 0 = The clock is required.
PCIE_PERST_L	W14	I (PU)	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification (3.3V i/f).
PCIE_PME_L	W16	OD	PCI power management event. Used to request a change in the device or system power state. The assertion and deassertion of PCI_PME are asynchronous to PCI_CLK. This signal has an open-drain output structure, as per the PCI Bus Local Bus Specification, revision 2.3. (3.3V i/f).
RDP0	D19	I	Receiver differential pair Lane 0
RDN0	D18	I	
TDP0	E17	O	Transmitter differential pair Lane 0
TDN0	D17	O	
RDP1	A17	I	Receiver differential pair Lane 1
RDN1	A18	I	

Table 4: Signal Descriptions

Signal	*284-pin ERFCBGA*	*Type*	*Description*
TDP1	A15	O	Transmitter differential pair Lane 1
TDN1	B15	O	
REFCLKP	F18	I	PCIE differential reference clock input (negative and positive). 100 MHz differential.
REFCLKN	F19	O	–
TESTP	D13	–	PCIe test pin. Do not connect anything to this pin.
TESTN	E13	O	
RF Control Interface			
C0_FEMCTRL_0/FEMCTRL_0	B5	O	RF Front End controls for Core 0
C0_FEMCTRL_1/FEMCTRL_1	D5	O	RF Front End controls for Core 0
C0_FEMCTRL_2/FEMCTRL_2	E5	O	RF Front End controls for Core 0
C0_FEMCTRL_3/FEMCTRL_12	A8	O	RF Front End controls for Core 0
C1_FEMCTRL_0/FEMCTRL_3	A5	O	RF Front End controls for Core 1
C1_FEMCTRL_1/FEMCTRL_4	A6	O	RF Front End controls for Core 1
C1_FEMCTRL_2/FEMCTRL_5	B6	O	RF Front End controls for Core 1
C1_FEMCTRL_3/FEMCTRL_13	B8	O	RF Front End controls for Core 1
C2_FEMCTRL_0/FEMCTRL_6	D6	O	RF Front End controls for Core 2
C2_FEMCTRL_1/FEMCTRL_7	E6	O	RF Front End controls for Core 2
C2_FEMCTRL_2/FEMCTRL_8	E7	O	RF Front End controls for Core 2
C2_FEMCTRL_3/FEMCTRL_14	D8	O	RF Front End controls for Core 2
C3_FEMCTRL_0/FEMCTRL_9	D7	O	RF Front End controls for Core 3
C3_FEMCTRL_1/FEMCTRL_10	B7	O	RF Front End controls for Core 3
C3_FEMCTRL_2/FEMCTRL_11	A7	O	RF Front End controls for Core 3
C3_FEMCTRL_3/FEMCTRL_15	E8	O	RF Front End controls for Core 3
RF_DISABLE_L	T12	I	RF disable. When asserted, disables the internal radio and shuts off everything except the crystal oscillator.
RF Signal Interface			
RF2G_IN_C0	C1	I	Core 0 RF receive input, 2.4 GHz band
RF2G_IN_C1	H1	I	Core 1 RF receive input, 2.4 GHz band
RF2G_IN_C2	N1	I	Core 1 RF receive input, 2.4 GHz band
RF2G_IN_C3	V1	I	Core 1 RF receive input, 2.4 GHz band
RF5G_IN_C0	B1	I	Core 0 RF receive input, 5 GHz band
RF5G_IN_C1	G1	I	Core 1 RF receive input, 5 GHz band
RF5G_IN_C2	M1	I	Core 2 RF receive input, 5 GHz band
RF5G_IN_C3	U1	I	Core 3 RF receive input, 5 GHz band
RF2G_OUT_C0	D2	O	Core 0 RF transmit output, 2.4 GHz band
RF2G_OUT_C1	J2	O	Core 1 RF transmit output, 2.4 GHz band
RF2G_OUT_C2	P2	O	Core 2 RF transmit output, 2.4 GHz band

Table 4: Signal Descriptions

Signal	*284-pin ERFCBGA*	*Type*	*Description*
RF2G_OUT_C3	W2	O	Core 3 RF transmit output, 2.4 GHz band
RF5G_OUT_C0	A2	O	Core 0 RF transmit output, 5GHz band
RF5G_OUT_C1	F2	O	Core 1 RF transmit output, 5 GHz band
RF5G_OUT_C2	P2	O	Core 2 RF transmit output, 5 GHz band
RF5G_OUT_C3	T2	O	Core 3 RF transmit output, 5 GHz band
TSSI_C0	C4	I	TSSI input from power detector, Core 0.
TSSI_C1	D4	I	TSSI input from power detector, Core 1.
TSSI_C2	R4	I	TSSI input from power detector, Core 2.
TSSI_C3	T3	I	TSSI input from power detector, Core 3.
GPAIO_I	B16	I/O	General-purpose analog I/O.
RCAL_EXT_RES/ RADIO_TEST_1	L3	I/O	External RCAL resistor connection. Connect a 10.0 kΩ, 1%, resistor from this pin to ground. Multiplexed with general-purpose analog I/O.
RADIO_TEST_2	M3	I/O	Multiplexed with general-purpose analog I/O. Do not connect
RADIO_TEST_3	M4	I/O	Multiplexed with general-purpose analog I/O. Do not connect
RADIO_TEST_4	L4	I/O	Multiplexed with general-purpose analog I/O. Do not connect
JTAG Interface			
GPIO_0/TRST_L	W12	O	JTAG reset output. Resets the JTAG Controller. If not used, it may be left unconnected. This pin is multiplexed with: • GPIO 0
GPIO_1/TCK/SWD_CLK	V12	I	JTAG test clock input. Used to synchronize JTAG control and data transfers. If not used, it may be left unconnected. This pin is multiplexed with: • GPIO 1 • SWD_CLK
GPIO_2/TDO	R11	O	JTAG test data output. Serial data output from the JTAG TAP controller. Output on the rising edge of TCK. If not used, it may be left unconnected. This pin is multiplexed with: • GPIO 2
GPIO_3/TDI	T11	I	JTAG test data input. Serial data input to the JTAG TAP controller. Sampled on the rising edge of TCK. If not used, it may be left unconnected. This pin is multiplexed with: • GPIO 3

Table 4: Signal Descriptions

Signal	*284-pin ERFCBGA*	*Type*	*Description*
GPIO_4/TMS/SWD_DATA	W10	I	JTAG Mode Select Input. Single control input to the JTAG TAP controller used to traverse the test logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected. This pin is multiplexed with: • GPIO 4 • SWD_DATA
JTAG_SELECT	T14	I	JTAG Select. When set low, the GPIO_[4:0] and GPIO_10 pins are set to use their normal GPIO functions. When set high, the GPIO_[4:0] pins are used as JTAG pins, and the GPIO_10 pin is used as EXT_POR_L.
GPIO Interface			
GPIO_5/SWD_CLK	V10	I/O	GPIO 5, general-purpose I/O. This pin is multiplexed with the ARM SWD_CLK signal.
GPIO_6/SWD_DATA	U10	I/O	GPIO 6, general-purpose I/O. This pin is multiplexed with the ARM SWD_DATA signal.
GPIO_7/UART_RX	R10	I/O	GPIO 7, general-purpose I/O. This pin is also multiplexed with the UART receive signal, UART_RX.
GPIO_8/UART_TX	T10	I/O	GPIO 8, general-purpose I/O. This pin is also multiplexed with the UART transmit signal, UART_TX.
GPIO_9	R8	I/O	GPIO 9, general-purpose I/O.
GPIO_10/EXT_POR_L	R9	I/O	GPIO 10, general-purpose I/O. When JTAG_SEL is pulled high, this pin becomes the EXT_POR_L input.
GPIO_11	T9	I/O	GPIO 11, general-purpose I/O.
GPIO_12	T8	I/O	GPIO 12, general-purpose I/O.
GPIO_13	U8	I/O	GPIO 13, general-purpose I/O.
GPIO_14	V8	I/O	GPIO 14, general-purpose I/O.
GPIO_15	W8	I/O	GPIO 15, general-purpose I/O.
RF_DISABLE	T12	I	When made '1' RF circuit is disabled
BSC_SDA	U12	I/0	BBS test interface
BSC_SCL	T13	I/O	BBS test interface
TRACE_0	A9	O	Bit 0, digital ARM/PHY test interface
TRACE_1	H9	O	Bit 1, digital ARM/PHY test interface
TRACE_2	B9	O	Bit 2, digital ARM/PHY test interface
TRACE_3	C9	O	Bit 3, digital ARM/PHY test interface
TRACE_4	D9	O	Bit 4, digital ARM/PHY test interface
TRACE_5	E9	O	Bit 5, digital ARM/PHY test interface
TRACE_6	H10	O	Bit 6, digital ARM/PHY test interface
TRACE_7	B12	O	Bit 7, digital ARM/PHY test interface

Table 4: Signal Descriptions

Signal	*284-pin ERFCBGA*	*Type*	*Description*
TRACE_8	A12	O	Bit 8, digital ARM/PHY test interface
TRACE_9	C12	O	Bit 9, digital ARM/PHY test interface
TRACE_10	H11	O	Bit 10, digital ARM/PHY test interface
TRACE_11	F12	O	Bit 11, digital ARM/PHY test interface
TRACE_12	D12	O	Bit 12, digital ARM/PHY test interface
TRACE_13	E12	O	Bit 13, digital ARM/PHY test interface
TRACE_14	H12	O	Bit 14, digital ARM/PHY test interface
TRACE_15	G12	O	Bit 15, digital ARM/PHY test interface
TRACCLK	G9	O	Clock, 133 MHz, digital ARM/PHY test interface
TRACECTL	F9	O	Control, digital ARM/PHY test interface
AVS			
STB_PVTMON_ADC	T16	I	AVS control circuit ADC input
STB_PVTMON_DAC	T17	O	AVS control circuit DAC output
AVDD_1P8	V16	Pwr	AVS supply 1.8V
VDD_SENSE	V18	O	Dedicated AVS supply sense pin for AVS and internal switcher
Internal AVS Switching Regulator			
PVDDIN_SW	P19	Pwr	Supply internal AVS switcher controller 2.5V–5 V. Bypass with 220 nF to ground right below the respective ball on PCB. Tie to ground to disable regulator.
AVDDIN_SW	W19	Pwr	Analog 2.5V to 5.0V input. Bypass with 1 µF to ground Tie to ground for disabled regulator.
VDD_DIG_SENSE_SW	V19	I	Voltage sense feedback. Tie to ground for disabled regulator.
SWREG_DIS	U14	I	1MEG internal pull-down. Open or tie to ground: Enable internal switcher regulator. High: Disable internal regulator.
SENSE_SW	U19	I	Overcurrent protection high-side sense. Add 1K minimum external resistor on PCB, and optional filtering cap 10–100 pF. Tie to ground for disable regulator.
PDRIVE_SW	T19	O	Drive signal for internal switcher controller external P-MOSFET.
NDRIVE_SW	R19	O	Drive signal for internal switcher controller external N-MOSFET

Table 4: Signal Descriptions

Signal	*284-pin ERFCBGA*	*Type*	*Description*
Power and Ground			
VDD	H16, H17, H18, H19, H6, H7, H8, J12, J13, J14, J17, J18, J7, J8, K10, K15, K16, K19, K5, K6, K9, L10, L11, L15, L16, L19, L5, L6, L9, M11, M13, M14, M17, M18, M7, M8, N13, N17, N18, P13, P14, V18	Pwr	0.95–1.05V AVS supply input for the core logic (ARM, PHY, SerDes, MEM, WL).
VDDO_V3P3	G6, P11	Pwr	3.3V supply input for digital I/O: ext SROM, PCIE, radio control signals FEM_CTRL_0::15
VDDO_V1P8	G7, G8, N10, N11	Pwr	1.8V supply input for digital I/O, TRACE_0::15, TRACECTL, TRACECLK, and internal SROM
MULTI_VDDO_SET_3P3	P9	I	Configures internal GPIO pads to supply voltage used: • VDDO_MULTI uses 3.3V: connect this pin to VDDO_V3P3. • VDDO_MULTI uses 1.8V: connect this pin to GND.
VDDO_MULTI	P10	Pwr	1.8V or 3.3V supply input for GPIO_0:: 15/ JTAG
PCIE_VDD_1P8	C14	Pwr	1.8V input for on-chip PCIe LDO
PCIE_LDO_IN_1P2	F14	Pwr	1.2V input for on-chip PCIe LDO
PCIE_LDO_OUT_1P0	D14	Pwr	1.0V PCIe LDO output
PCIE_LDO_SENSE	E14	I	1.0V PCIe LDO sense input
TVDD1P0	E16	Pwr	PCIe SerDes 1.0V supply input
PVDD1P0	F16	Pwr	PCIe SerDes 1.0V supply input
RVDD1P0	F17	Pwr	PCIe SerDes 1.0V supply input
BBPLL_PAD_VDD1P8	L12	Pwr	BB (PHY) PLL Synthesizer supply 1.8V
CPUPLL_PAD_VDD1P8	N16	Pwr	CPU (ARM) PLL Synthesizer supply 1.8V
SYNTH0_VDD3P3	B18	Pwr	Synthesizer supply input 3.3V.
SYNTH_VDD_V1P22V_SYNTH0	P6	Pwr	Radio synthesizer 0 supply input 1.22V
SYNTH_VDD_V1P22V_SYNTH1	U4	Pwr	Radio synthesizer 1 supply input 1.22V
SYNTH_VDD_V3P3V_SYNTH0	R7	Pwr	Radio synthesizer 0 supply input 3.3V
SYNTH_VDD_V3P3V_SYNTH1	V4	Pwr	Radio synthesizer 1 supply input 3.3V

Table 4: Signal Descriptions

Signal	*284-pin ERFCBGA*	*Type*	*Description*
VCOBUF_VDD_V1P22V_SYNTH0	P7	Pwr	Radio VCO buffer 0 supply input 1.22V
VCOBUF_VDD_V1P22V_SYNTH1	R5	Pwr	Radio VCO buffer 1 supply input 1.22V
WIFI_TX_VDD1_V1P8	C3	Pwr	Radio TX supply 1.8V
WIFI_TX_VDD0_V1P8	U3	Pwr	Radio TX supply 1.8V
WIFI_MIX_VDD1_V1P8	E3	Pwr	Radio mixer supply 1.8V
WIFI_MIX_VDD0_V1P8	V3	Pwr	Radio mixer supply 1.8V
WIFI_PMU_VDD_V1P2_0	F3	Pwr	Radio PMU input 1.22V
WIFI_PMU_VDD_V1P2_1	G4	Pwr	Radio PMU input 1.22V
WIFI_PMU_VDD_V1P2_2	R3	Pwr	Radio PMU input 1.22V
WIFI_PMU_VDD_V1P8	T4	Pwr	Radio PMU input 1.8V
WIFI_PMU_VDD_V3P3	P5	Pwr	Radio PMU input 3.3V
WRF_XTAL_VDD_V1P8	U7	Pwr	Crystal oscillator internal LDO input 1.8V
VSS	A13, A14, A16, A19, A3, A4, B10, B11, B13, B14, B16, B17, B18, B19, B2, B4, C13, C15, C2, D10, D11, D15, D16, D3, E15, E4, F10, F11, F13, F4, G13, G17, G18, G19, G2, G5, H15, H2, H3, H4, H5, J10, J11, J15, J16, J19, J4, J5, J6, J9, K11, K12, K13, K14, K17, K18, K4, K7, K8, L13, L14, L17, L18, L7, L8, M10, M12, M15, M16, M19, M2, M5, M6, M9, N14, N19, N2, N4, N5, N9, P16, P17, P18, P4, T18, U11, U16, U18, U2, V13, V2, V9, W11, W3	Pwr	Ground/VSS

Strapping Options

The pins listed in the table below are sampled at Power-On Reset (POR) to determine the various operating modes. Sampling occurs within a few milliseconds following internal POR or deassertion of external POR. After POR, each pin assumes the function specified in the signal descriptions table. Each pin has an internal Pull-Up (PU) or Pull-Down (PD) resistor that determines the default mode. To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND-use 10 kΩ or less (refer to the reference board schematics for further details).

Table 5: Strapping Options[a]

Signal Name	*Mode*	*Default*	*Description*
GPIO_5/	–	PD	0: Use radio XTAL. 1: Bypass radio XTAL.
GPIO_6/	SWD Mode	PU	0: No SPROM 1: SPROM is present
GPIO_8	SPROM size select	PU	0: 64 Kb (default). 1: 16 Kb.
SPROM_DOUT	SWD on JTAG	PD	0: ARM SWD port not muxed onto JTAG pins. 1: ARM SWD port muxed onto JTAG pins. SWD works on JTAG interface GPIO1 (TCK) and GPIO4 (TMS).
SWREG_DIS	Disable internal AVS switcher controller circuit	Open	Open: Use internal AVS switcher controller. 0: Short to gnd, disabled (and gnd some other pins, see "AVS" on page 37)

a. These functions are controlled by the strapping option and the driver. These pins should be strapped as shown in the appropriate Broadcom reference board schematic.

Section 5: RF Specifications

Introduction

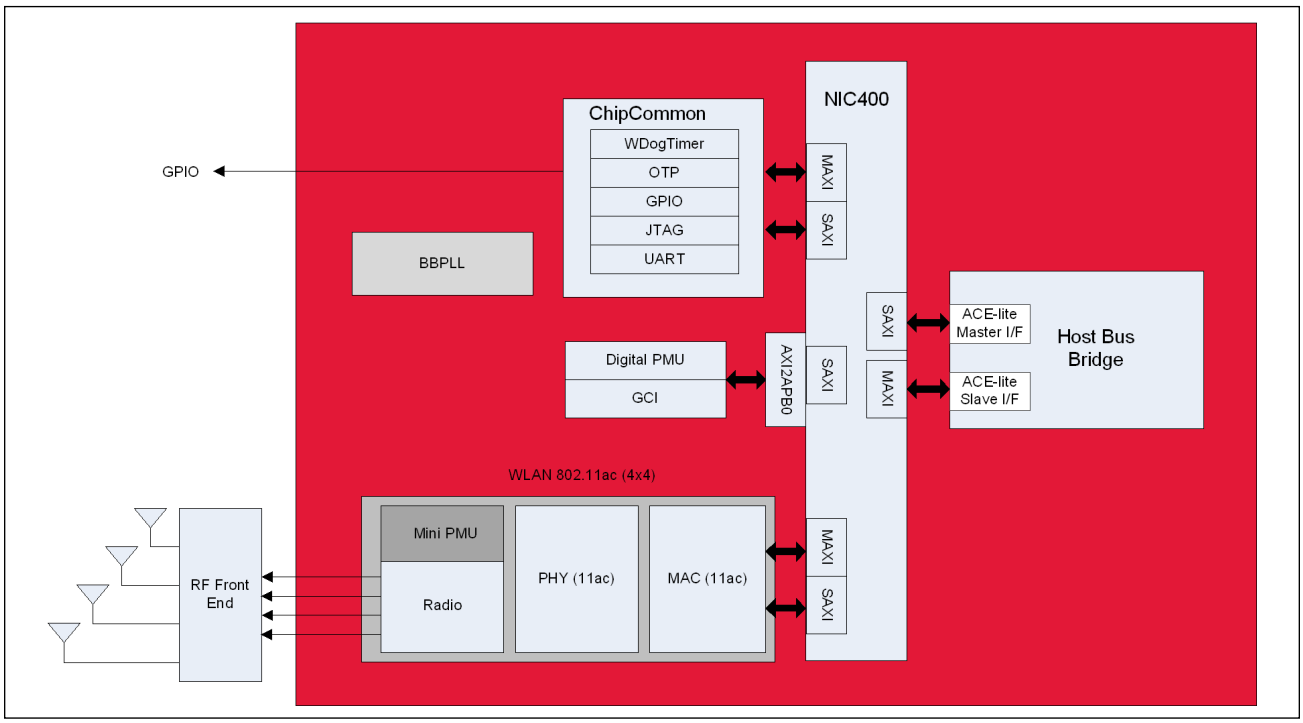
The BCM43684 includes an integrated dual-band direct conversion radio that supports either the 2.4 GHz band or the 5 GHz band. This section describes the RF characteristics of the 2.4 GHz and 5 GHz portions of the radio.

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

WLAN

A functional block diagram of the BCM43684 WLAN is shown in the following figure.

Figure 9: WLAN Block Diagram



Note: The BCM43684 has a total of four WLAN ports.

2.4 GHz Band General RF Specifications

Table 6: 2.4 GHz Band General RF Specifications

Item	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
TX/RX switch time	Including TX ramp down	–	–	5	µs
RX/TX switch time	Including TX ramp up	–	–	2	µs
Power-up and power-down ramp time	DSSS/CCK modulations	–	–	< 2	µs

WLAN 2.4 GHz Receiver Performance Specifications

Note: All values in the following table are preliminary and subject to change.

Table 7: WLAN 2.4 GHz Receiver Performance Specifications

Parameter	*Condition/Notes*	*Min.*	*Typ.*	*Max.*	*Unit*
Frequency range	–	2400	–	2500	MHz
IEEE 802.11b RX sensitivity (8% PER for 1024 octet PSDU)	1 Mb/s DSSS	–	tbd	–	dBm
	2 Mb/s DSSS	–	tbd	–	dBm
	5.5 Mb/s DSSS	–	tbd	–	dBm
	11 Mb/s DSSS	–	tbd	–	dBm
IEEE 802.11g RX sensitivity (10% PER for 1024 octet PSDU)	6 Mb/s OFDM	–	tbd	–	dBm
	9 Mb/s OFDM	–	tbd	–	dBm
	12 Mb/s OFDM	–	tbd	–	dBm
	18 Mb/s OFDM	–	tbd	–	dBm
	24 Mb/s OFDM	–	tbd	–	dBm
	36 Mb/s OFDM	–	tbd	–	dBm
	48 Mb/s OFDM	–	tbd	–	dBm
	54 Mb/s OFDM	–	tbd	–	dBm

Table 7: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*	*Min.*	*Typ.*	*Max.*	*Unit*
IEEE 802.11n RX sensitivity (10% PER for 4096 octet PSDU)[a]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	**20 MHz channel spacing for all MCS rates**				
	MCS 15	tbd	tbd	–	dBm
	MCS 8	tbd	tbd	–	dBm
	MCS 7	tbd	tbd	–	dBm
	MCS 6	tbd	tbd	–	dBm
	MCS 5	tbd	tbd	–	dBm
	MCS 4	tbd	tbd	–	dBm
	MCS 3	tbd	tbd	–	dBm
	MCS 2	tbd	tbd	–	dBm
	MCS 1	tbd	tbd	–	dBm
	MCS 0	tbd	tbd	–	dBm
	40 MHz channel spacing for all MCS rates				
	MCS 15	tbd	tbd	–	dBm
	MCS 8	tbd	tbd	–	dBm
	MCS 7	tbd	tbd	–	dBm
	MCS 6	tbd	tbd	–	dBm
	MCS 5	tbd	tbd	–	dBm
	MCS 4	tbd	tbd	–	dBm
	MCS 3	tbd	tbd	–	dBm
	MCS 2	tbd	tbd	–	dBm
	MCS 1	tbd	tbd	–	dBm
	MCS 0	tbd	tbd	–	dBm
IEEE 802.11ac RX sensitivity (10% PER for 4096 octet PSDU). Defined for default parameters: GF, 800 ns GI, and non-STBC.	**20 MHz channel spacing for all MCS rates**				
	MCS 9	tbd	tbd	–	dBm
	MCS 8	tbd	tbd	–	dBm
	MCS 7	tbd	tbd	–	dBm
	MCS 6	tbd	tbd	–	dBm
	MCS 5	tbd	tbd	–	dBm
	MCS 4	tbd	tbd	–	dBm
	MCS 3	tbd	tbd	–	dBm
	MCS 2	tbd	tbd	–	dBm
	MCS 1	tbd	tbd	–	dBm
	MCS 0	tbd	tbd	–	dBm

Table 7: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*	*Min.*	*Typ.*	*Max.*	*Unit*
IEEE 802.11ac RX sensitivity (10% PER for 4096 octet PSDU)[a]. Defined for default parameters: GF, 800 ns GI, and non-STBC.	**40 MHz channel spacing for all MCS rates**				
	MCS11	tbd	tbd	–	dBm
	MCS10	tbd	tbd	–	dBm
	MCS 9	tbd	tbd	–	dBm
	MCS 8	tbd	tbd	–	dBm
	MCS 7	tbd	tbd	–	dBm
	MCS 6	tbd	tbd	–	dBm
	MCS 5	tbd	tbd	–	dBm
	MCS 4	tbd	tbd	–	dBm
	MCS 3	tbd	tbd	–	dBm
	MCS 2	tbd	tbd	–	dBm
	MCS 1	tbd	tbd	–	dBm
	MCS 0	tbd	tbd	–	dBm
In-band static CW jammer immunity (fc - 8 MHz < fcw < + 8 MHz)	RX PER < 1%, 54 Mb/s OFDM, 1000 octet PSDU for: (RxSens + 23 dB < Rxlevel < max input level)	tbd			dBm
Input In-Band IP3	Maximum LNA gain	–	tbd	–	dBm
	Minimum LNA gain	–	tbd	–	dBm
Maximum Receive Level @ 2.4 GHz	@ 1, 2 Mb/s (8% PER, 1024 octets)	tbd	–	–	dBm
	@ 5.5, 11 Mb/s (8% PER, 1024 octets)	tbd	–	–	dBm
	@ 6-54 Mb/s (10% PER, 1024 octets)	tbd	–	–	dBm
	@ MCS 0 through 7 rates (10% PER, 4095 octets)	tbd	–	–	dBm
LPF 3 dB Bandwidth	–	tbd	–	–	MHz
IEEE 802.11b Adjacent channel rejection-DSSS (Difference between interfering and desired signal at 8% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	**Desired and interfering signal 30 MHz apart**				
	1 Mb/s DSSS	tbd	tbd	–	dB
	2 Mb/s DSSS	tbd	tbd	–	dB
	Desired and interfering signal 25 MHz apart				
	5.5 Mb/s DSSS	tbd	tbd	–	–
	11 Mb/s DSSS	tbd	tbd	–	–
IEEE 802.11g Adjacent channel rejection-OFDM (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 1024 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mb/s OFDM	tbd	tbd	–	–
	9 Mb/s OFDM	tbd	tbd	–	–
	12 Mb/s OFDM	tbd	tbd	–	–
	18 Mb/s OFDM	tbd	tbd	–	–
	24 Mb/s OFDM	tbd	tbd	–	–
	36 Mb/s OFDM	tbd	tbd	–	–
	48 Mb/s OFDM	tbd	tbd	–	–
	54 Mb/s OFDM	tbd	tbd	–	–

Table 7: WLAN 2.4 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
IEEE 802.11n Adjacent channel rejection MCS0 to MCS7 (Difference between interfering and desired signal (25 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/ Notes)	MCS7	tbd	tbd	–	–
	MCS6	tbd	tbd	–	–
	MCS5	tbd	tbd	–	–
	MCS4	tbd	tbd	–	–
	MCS3	tbd	tbd	–	–
	MCS2	tbd	tbd	–	–
	MCS1	tbd	tbd	–	–
	MCS0	tbd	tbd	–	–
IEEE 802.11ac Adjacent channel rejection MCS0 to MCS9 (Difference between interfering and desired signal at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/ Notes)	MCS9	tbd	tbd	–	–
	MCS8	tbd	tbd	–	–
	MCS7	tbd	tbd	–	–
	MCS6	tbd	tbd	–	–
	MCS5	tbd	tbd	–	–
	MCS4	tbd	tbd	–	–
	MCS3	tbd	tbd	–	–
	MCS2	tbd	tbd	–	–
	MCS1	tbd	tbd	–	–
	MCS0	tbd	tbd	–	–
Maximum receiver gain	–	–	tbd	–	dB
Gain control step	–	–	tbd	–	dB
RSSI accuracy[b]	Range –98 dBm to –30 dBm	–5	–	5	dB
	Range above –30 dBm	–8	–	8	dB
Return loss	Zo = 50Ω, across the dynamic range	tbd	tbd	tbd	dB
Receiver cascaded noise figure	At maximum gain	–	tbd	–	–

a. Sensitivity degradations for alternate settings in MCS modes.
MM: 0.5 dB drop, SGI: 2 dB drop, STBC: 0.75 dB drop.
b. The minimum and maximum values shown have a 95% confidence level.

WLAN 2.4 GHz Transmitter Performance Specifications

Note: All values in the following table are preliminary and subject to change.

Table 8: WLAN 2.4 GHz Transmitter Performance Specifications

Parameter	Condition/Notes		Min.	Typ.	Max.	Units
Frequency range	–		2400	–	2500	MHz
Harmonic level (at –5 dBm with 100% duty cycle)	4.8–5.0 GHz	2nd harmonic	–	tbd	–	dBm/ 1 MHz
	7.2–7.5 GHz	3rd harmonic	–	tbd	–	dBm/ 1 MHz
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance[a]	IEEE 802.11b (DSSS/CCK)	–9 dB	–	tbd	–	dBm
	OFDM, BPSK	–8 dB	–	tbd	–	dBm
	OFDM, QPSK	–13 dB	–	tbd	–	dBm
	OFDM, 16-QAM	–19 dB	–	tbd	–	dBm
	OFDM, 64-QAM (R = 3/4)	–25 dB	–	tbd	–	dBm
	OFDM, 64-QAM (R = 5/6)	–28 dB	–	tbd	–	dBm
	OFDM, 256-QAM (R = 3/4, VHT20)	–30 dB	–	tbd	–	dBm
	OFDM, 256-QAM (R = 5/6, VHT20)	–32 dB	–	tbd	–	dBm
	OFDM, 1024-QAM (R = 3/4 VHT20)	–34 dB	–	tbd	–	dBm
	OFDM, 1024-QAM (R = 5/6 VHT20)	–35 dB	–	tbd	–	dBm
Phase noise	40 MHz crystal, Integrated from 10 kHz to 10 MHz		–	tbd	–	Degrees
TX power control dynamic range	–		tbd	–	–	dB
Carrier suppression	–		15	–	–	dBc
Gain control step	–		–	0.25	–	dB
Return loss at Chip port TX	Zo = 50Ω		–	tbd	–	dB

a. TX power for Channel 1 and Channel 11 is specified by nonvolatile memory parameters.

WLAN 5 GHz Receiver Performance Specifications

Note: All values in the following table are preliminary and subject to change.

Table 9: WLAN 5 GHz Receiver Performance Specifications

Parameter	*Condition/Notes*	*Min.*	*Typ.*	*Max.*	*Units*
Frequency range	–	4900	–	5925	MHz
IEEE 802.11a RX sensitivity	6 Mb/s OFDM	–	tbd	–	dBm
(10% PER for 1000 octet PSDU)	9 Mb/s OFDM	–	tbd	–	dBm
	12 Mb/s OFDM	–	tbd	–	dBm
	18 Mb/s OFDM	–	tbd	–	dBm
	24 Mb/s OFDM	–	tbd	–	dBm
	36 Mb/s OFDM	–	tbd	–	dBm
	48 Mb/s OFDM	–	tbd	–	dBm
	54 Mb/s OFDM	–	tbd	–	dBm
IEEE 802.11n RX sensitivity	**20 MHz channel spacing for all MCS rates**				
(10% PER for 4096 octet PSDU)	MCS 15	–	tbd	–	dBm
Defined for default parameters: GF, 800 ns GI, and non-STBC.	MCS 8	–	tbd	–	dBm
	MCS 7	–	tbd	–	dBm
	MCS 6	–	tbd	–	dBm
	MCS 5	–	tbd	–	dBm
	MCS 4	–	tbd	–	dBm
	MCS 3	–	tbd	–	dBm
	MCS 2	–	tbd	–	dBm
	MCS 1	–	tbd	–	dBm
	MCS 0	–	tbd	–	dBm
	40 MHz channel spacing for all MCS rates				
	MCS 15	–	tbd	–	dBm
	MCS 8	–	tbd	–	dBm
	MCS 7	–	tbd	–	dBm
	MCS 6	–	tbd	–	dBm
	MCS 5	–	tbd	–	dBm
	MCS 4	–	tbd	–	dBm
	MCS 3	–	tbd	–	dBm
	MCS 2	–	tbd	–	dBm
	MCS 1	–	tbd	–	dBm
	MCS 0	–	tbd	–	dBm

Table 9: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	*Condition/Notes*	*Min.*	*Typ.*	*Max.*	*Units*
IEEE 802.11ac RX sensitivity (10% PER for 4096 octet PSDU) Defined for default parameters: GF, 800 ns GI, and non-STBC.	**20 MHz channel spacing for all MCS rates**				
	MCS 8	tbd	tbd	–	dBm
	MCS 7	tbd	tbd	–	dBm
	MCS 6	tbd	tbd	–	dBm
	MCS 5	tbd	tbd	–	dBm
	MCS 4	tbd	tbd	–	dBm
	MCS 3	tbd	tbd	–	dBm
	MCS 2	tbd	tbd	–	dBm
	MCS 1	tbd	tbd	–	dBm
	MCS 0	tbd	tbd	–	dBm
	40 MHz channel spacing for all MCS rates				
	MCS11	tbd	tbd	–	dBm
	MCS10	tbd	tbd	–	dBm
	MCS 9	tbd	tbd	–	dBm
	MCS 8	tbd	tbd	–	dBm
	MCS 7	tbd	tbd	–	dBm
	MCS 6	tbd	tbd	–	dBm
	MCS 5	tbd	tbd	–	dBm
	MCS 4	tbd	tbd	–	dBm
	MCS 3	tbd	tbd	–	dBm
	MCS 2	tbd	tbd	–	dBm
	MCS 1	tbd	tbd	–	dBm
	MCS 0	tbd	tbd	–	dBm
	80 MHz channel spacing for all MCS rates				
	MCS11	tbd	tbd	–	dBm
	MCS10	tbd	tbd	–	dBm
	MCS 9	tbd	tbd	–	dBm
	MCS 8	tbd	tbd	–	dBm
	MCS 7	tbd	tbd	–	dBm
	MCS 6	tbd	tbd	–	dBm
	MCS 5	tbd	tbd	–	dBm
	MCS 4	tbd	tbd	–	dBm
	MCS 3	tbd	tbd	–	dBm
	MCS 2	tbd	tbd	–	dBm
	MCS 1	tbd	tbd	–	dBm
	MCS 0	tbd	tbd	–	dBm
Input In-Band IP3	Maximum LNA gain	–	tbd	–	dBm
	Minimum LNA gain	–	tbd	–	dBm

Table 9: WLAN 5 GHz Receiver Performance Specifications (Cont.)

Parameter	Condition/Notes		Min.	Typ.	Max.	Units
Maximum receive level @ 5.24 GHz	@ 6, 9, 12 Mb/s		tbd	–	–	dBm
	@ 18, 24, 36, 48, 54 Mb/s		tbd	–	–	dBm
LPF 3 dB bandwidth	–		tbd	–	–	MHz
Adjacent channel rejection (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as specified in Condition/Notes)	6 Mb/s OFDM	tbd	tbd	–	–	dB
	9 Mb/s OFDM	tbd	tbd	–	–	dB
	12 Mb/s OFDM	tbd	tbd	–	–	dB
	18 Mb/s OFDM	tbd	tbd	–	–	dB
	24 Mb/s OFDM	tbd	tbd	–	–	dB
	36 Mb/s OFDM	tbd	tbd	–	–	dB
	48 Mb/s OFDM	tbd	tbd	–	–	dB
	54 Mb/s OFDM	tbd	tbd	–	–	dB
Alternate adjacent channel rejection (Difference between interfering and desired signal (40 MHz apart) at 10% PER for 1000[a] octet PSDU with desired signal level as specified in Condition/Notes)	6 Mb/s OFDM	tbd	tbd	–	–	dB
	9 Mb/s OFDM	tbd	tbd	–	–	dB
	12 Mb/s OFDM	tbd	tbd	–	–	dB
	18 Mb/s OFDM	tbd	tbd	–	–	dB
	24 Mb/s OFDM	tbd	tbd	–	–	dB
	36 Mb/s OFDM	tbd	tbd	–	–	dB
	48 Mb/s OFDM	tbd	tbd	–	–	dB
	54 Mb/s OFDM	tbd	tbd	–	–	dB
IEEE 802.11ac Adjacent channel rejection MCS0 to MCS9 (Difference between interfering and desired signal at 10% PER for 4096 octet PSDU with desired signal level as specified in Condition/ Notes)	MCS11		tbd	tbd	–	dBm
	MCS10		tbd	tbd	–	dBm
	MCS9	tbd	tbd	–	–	dB
	MCS8	tbd	tbd	–	–	dB
	MCS7	tbd	tbd	–	–	dB
	MCS6	tbd	tbd	–	–	dB
	MCS5	tbd	tbd	–	–	dB
	MCS4	tbd	tbd	–	–	dB
	MCS3	tbd	tbd	–	–	dB
	MCS2	tbd	tbd	–	–	dB
	MCS1	tbd	tbd	–	–	dB
	MCS0	tbd	tbd	–	–	dB
Maximum receiver gain	–		–	tbd	–	dB
Gain control step	–		–	tbd	–	dB
RSSI accuracy[b]	Range –98 dBm to –30 dBm		tbd	–	tbd	dB
	Range above –30 dBm		tbd	–	tbd	dB
Return loss	Zo = 50Ω		tbd	–	tbd	dB
Receiver cascaded noise figure	At maximum gain		–	tbd	–	dB

a. For 65 Mb/s, the size is 4096.
b. The minimum and maximum values shown have a 95% confidence level.

WLAN 5 GHz Transmitter Performance Specifications

Note: All values in the following table are preliminary and subject to change.

Table 10: WLAN 5 GHz Transmitter Performance Specifications

Parameter	*Condition/Notes*		*Min.*	*Typ.*	*Max.*	*Units*
Frequency range	–		4900	–	5925	MHz
Harmonic level (at –5 dBm)	9.8–11.570 GHz	2nd harmonic	–	tbd	–	dBm/ MHz
TX power at RF port for highest power level setting at 25°C with spectral mask and EVM compliance[a]	OFDM, QPSK	tbd	–	tbd	–	dBm
	OFDM, 16-QAM	tbd	–	tbd	–	dBm
	OFDM, 64-QAM (R = 3/4)	tbd	–	tbd	–	dBm
	OFDM, 64-QAM (R = 5/6)	tbd	–	tbd	–	dBm
	OFDM, 256-QAM (R = 3/4, VHT20)	tbd	–	tbd	–	dBm
	OFDM, 256-QAM (R = 5/6, VHT20)	tbd	–	tbd	–	dBm
	OFDM, 1024-QAM (R = 3/4 VHT20)	tbd	–	tbd	–	dBm
	OFDM, 1024-QAM (R = 5/6 VHT20)	tbd	–	tbd	–	dBm
Phase noise	40.0 MHz crystal, Integrated from 10 kHz to 10 MHz		–	tbd	–	Degrees
TX power control dynamic range	–		tbd	–	–	dB
Carrier suppression	–		tbd	–	–	dBc
Gain control step	–		–	tbd	–	dB
Return loss	Zo = 50Ω		–	tbd	–	dB

a. TX power is specified by nonvolatile memory parameters.

General Spurious Emissions Specifications

Table 11: General Spurious Emissions Specifications

Parameter	*Condition/Notes*		*Min.*	*Typ.*	*Max.*	*Units*
TX Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	tbd	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	tbd	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	tbd	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	tbd	–	dBm
RX/standby Emissions	30 MHz < f < 1 GHz	RBW = 100 kHz	–	tbd	–	dBm
	1 GHz < f < 12.75 GHz	RBW = 1 MHz	–	tbd	–	dBm
	1.8 GHz < f < 1.9 GHz	RBW = 1 MHz	–	tbd	–	dBm
	5.15 GHz < f < 5.3 GHz	RBW = 1 MHz	–	tbd	–	dBm

Section 6: Electrical Characteristics

Note: Values in this data sheet are design goals and are subject to change based on the results of device characterization.

Unless otherwise stated, limit values apply to the conditions specified in Table 12: “Absolute Maximum Ratings,” on page 52 and Table 13: “Recommended Operating Conditions,” on page 53. Typical values apply for an ambient temperature of +25°C.

Absolute Maximum Ratings

Caution! These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 12: Absolute Maximum Ratings

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Digital Core Supply Voltage[a]	VDD	VSS – 0.1	–	1.1	V
ARM, BB PLL Supply Voltage	[BB/CPU]_PAD_VDD	VSS – 0.18	–	1.98	V
1.8V I/O Supply Voltage	VDDx_1p8	VSS – 0.18	–	1.98	V
3.3V I/O Supply Voltage	VDDx_3p3	VSS – 0.33	–	3.63	V
Multi I/O Supply Voltage[b]	VDD_MULTIx	–	–	–	V
1.2V PCIe LDO Supply Voltage	PCIE_LDO_in	VSS – 0.12	–	1.98	V
1.8V PCIe LDO Supply Voltage	PCIE_LDO_in	VSS – 0.18	–	1.98	V
Xtal Oscillator Supply Voltage	WWRF_XTAL_VDD	VSS – 0.18	–	1.98	V
1.2V Radio Circuits	WIFI_VCOBUFx, WIFI_SYNTHx, WIFI_PMU	VSS - 0.12	-	1.32	V
1.8V Radio Circuits	WIFI_MIXx, WIFI_TXx, WIFI_PMU	VSS – 0.18	–	1.98	V
3.3V Radio Circuits	WIFI_SYNTHx, WIFI_PMU	VSS – 0.33	–	3.63	V
1.8 AVS Supply Circuits	AVDD_1P8	VSS – 0.3	–	1.98	V
Internal AVS Switcher Supply Voltage	AVDDIN_SW, PVDDIN_SW	VSS – 0.3	–	5.5	V
PCIe Differential Interface	TDx, RDx, REFCLKx	tbd	–	tbd	V

a. When automatic voltage scaling is not used.
b. When multi IP supply is 1.8V, use 1.8V I/O values. When multi supply is 3.3V, use 3.3V I/O values.

Recommended Operating Conditions and DC Characteristics

Table 13: Recommended Operating Conditions

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Digital Core Supply Voltage	VDD	0.95	1	1.05	V
ARM, BB PLL Supply Voltage	[BB/CPU]_PAD_VDD	1.71	1.8	1.89	V
1.8V I/O Supply Voltage	VDDx_1p8	1.71	1.8	1.89	V
3.3V I/O Supply Voltage	VDDx_3p3	3.135	3.3	3.465	V
Multi I/O Supply Voltage[a]	VDD_MULTIx	–	–	–	V
1.2V PCIe LDO Supply Voltage	PCIE_LDO_in	1.14	1.2	tbd	V
1.8V PCIe LDO Supply Voltage	PCIE_LDO_in	1.71	1.8	1.89	V
Xtal Oscillator Supply Voltage	WWRF_XTAL_VDD	1.71	1.8	1.89	V
1.2V Radio Circuits	WIFI_VCOBUFx, WIFI_SYNTHx, WIFI_PMU	1.14	1.2	1.26	V
1.8V Radio Circuits	WIFI_MIXx, WIFI_TXx, WIFI_PMU	1.71	1.8	1.89	V
3.3V Radio Circuits	WIFI_SYNTHx, WIFI_PMU	3.135	3.3	3.465	V
1.8 AVS supply Circuits	AVDD_1P8	1.71	1.8	1.89	V
Internal AVS Switcher Supply Voltage	AVDDIN_SW, PVDDIN_SW	2.5	3.3 / 5.0	5.5	V
PCIe Differential Interface	TDx, RDx, REFCLKx	tbd	–	tbd	V
Power Supply Ripple	Vripple	tbd	tbd	tbd	mVpp, 100 kHz–2 MHz
Digital Input High Voltage (3.3V)[b]	Vih	2	–	VDDO	V
Digital Input Low Voltage (3.3V)[b]	Vil	0	–	0.8	V
Digital Output High Voltage (3.3V)[b]	Vih	2.4	–	VDDO	V
Digital Output Low Voltage (3.3V)[b]	Vil	0	–	0.4	V
Digital Input High Voltage (1.8V)[b]	Voh	tbd	–	VDDO	V
Digital Input Low Voltage (1.8V)[b]	Vol	0	–	tbd	V
Digital Output High Voltage (1.8V)[b]	Voh	tbd	–	VDDO	V
Digital Output Low Voltage (1.8V)[b]	Vol	0	–	0.4	V
Operating Temperature and Supply Conditions					
Junction Temperature	Tj	–40	–	110[c]	°C
Ambient Temperature	Ta	–40	–	85[d]	°C

a. When multi IP supply is 1.8V, use 1.8V IO values. When multi supply is 3.3V, use 3.3V I/O values.
b. Values are typical and can vary dependent on output buffer configuration and load.
c. This is the maximum long-term junction temperature. Short-term excursions up to 125°C are allowed, with a maximum of 72 hours per year and 720 hours over the lifetime of the chip.
d. Maximum ambient temperature may need to be lower depending on used heat sink and airflow, in order to respect the maximum operating junction temperature.

Section 7: Timing Characteristics

Power Sequence Timing

Power-up of external 3.3V, 1.8V, 1.22V, and 1V (AVS) can be in any order within 20 ms total.

The power-up timing parameters are shown in Table 14.

Figure 10: Power-Up Sequence Timing Diagram

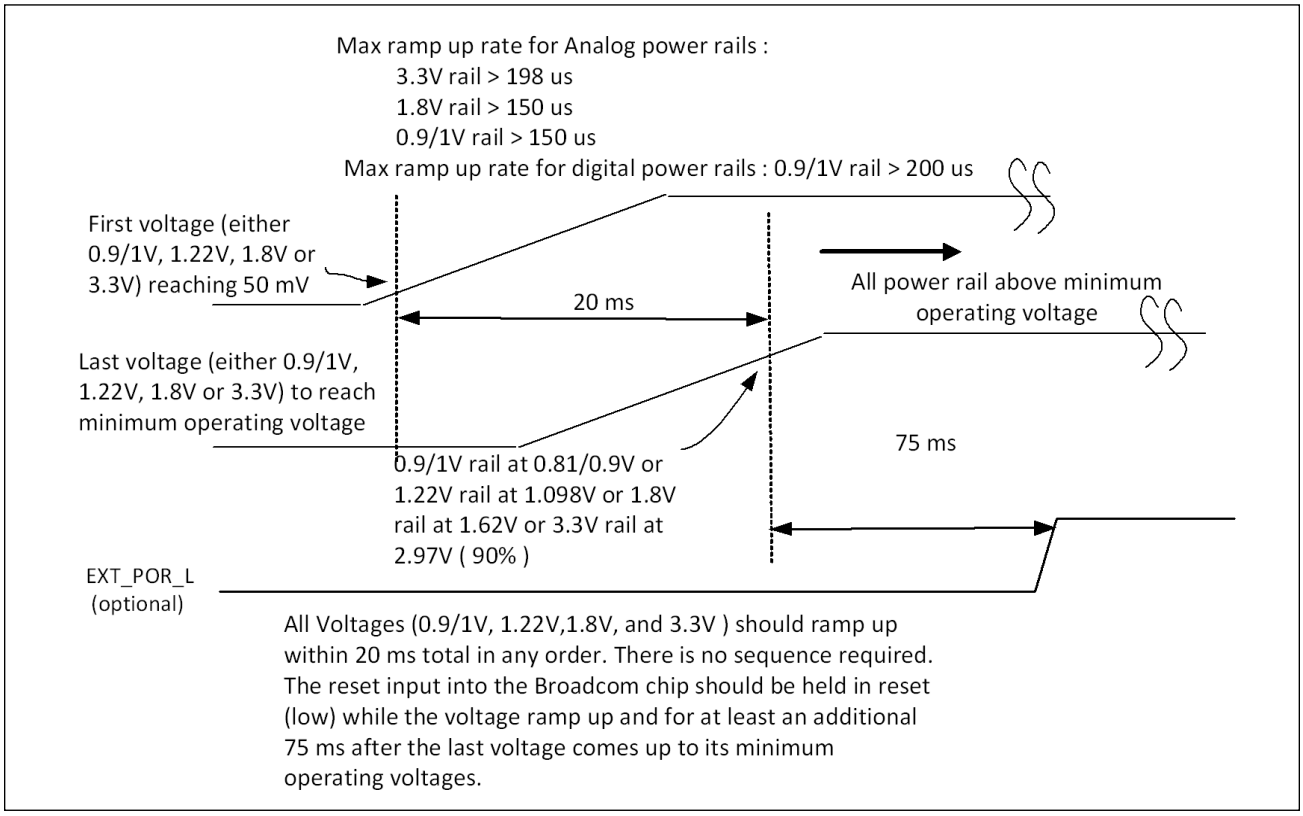


Table 14: Power-Up Timing Parameters

Symbol	Description	Min.	Typ.	Max.	Units
t_1	3.3V Active to 1.2V Active[a]	1	–	6.5	ms
t_2	Clock stable to reset deasserted[b]	5	–	–	ms
t_3	1.2V Active to reset deasserted[b]	40	–	–	ms
t_4	3.3V Active to 1.4V Active[a]	1	–	5.5	ms
t_5	1.4V Active to 1.2V Active[a]	1	–	5.5	ms

a. Power supply is considered Active when the supply has risen sufficiently to meet the Recommended Operating Conditions and DC Characteristics for that supply. For example, for 3.3V, the supply is Active when it is at least 3.135V.
b. Applies only if the EXT_POR_L input is used as a reset input.

SPROM Timing Diagram

Figure 11: SPROM Timing Diagram

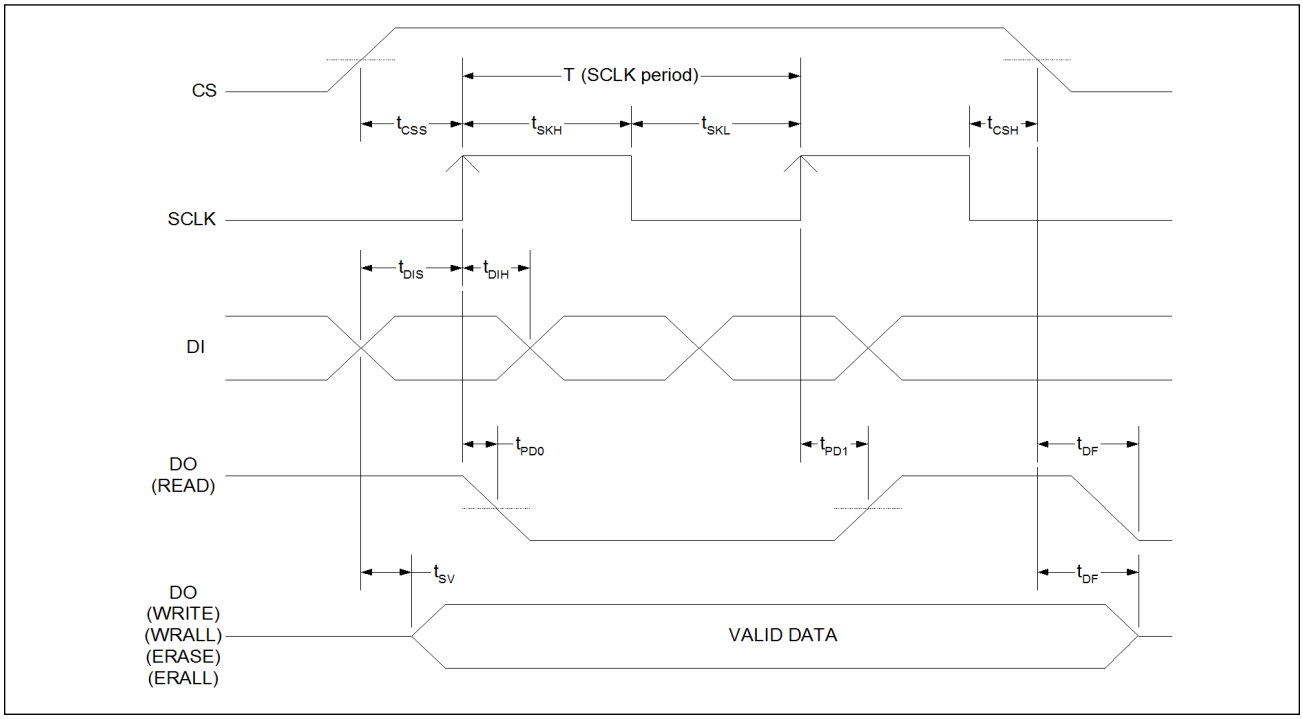


Table 15: SPROM Timing

Timing Symbol	*Parameter*	*Min.*	*Max.*	*Units*
f_{SK}	SCLK Clock Frequency	0	1	MHz
t_{SKH}	SCLK High Time	250	–	ns
t_{SKL}	SCLK Low Time	250	–	ns
t_{CS}	Minimum CS Low Time	250	–	ns
t_{CSS}	CS Setup Time	50	–	ns
t_{DIS}	DI Setup Time	100	–	ns
t_{CSH}	CS Hold Time	0	–	ns
t_{DIH}	DI Hold Time	100	–	ns
t_{PD0}	Output Delay to 1	–	500	ns
t_{PD1}	Output Delay to 0	–	500	ns
t_{SV}	CS to Data Valid	–	500	ns
t_{DF}	CS to DO in tristate	–	100	ns
t_{WP}	Write Cycle Time	–	10	ms

PCI Express Parameters

Table 16: PCI Express Parameters

Parameter	*Symbol*	*Comments*	*Min.*	*Typ.*	*Max.*	*Units*
General						
Baud rate	BPS	–	–	5	–	Gbaud
Reference clock amplitude	Vref	LVPECL, AC coupled	1	–	–	V
Receiver						
Differential termination	ZRX-DIFF-DC	Differential termination	80	100	120	Ω
DC impedance	ZRX-DC	DC common-mode impedance	40	50	60	Ω
Powered down termination (POS)	ZRX-HIGH-IMP-DC-POS	Power-down or RESET high impedance	100	–	–	kΩ
Powered down termination (NEG)	ZRX-HIGH-IMP-DC-NEG	Power-down or RESET high impedance	1	–	–	kΩ
Input voltage	VRX-DIFFp-p	AC coupled, differential p-p	175	–	–	mV
Jitter tolerance	TRX-EYE	Minimum receiver eye width	0.4	–	–	UI
Differential return loss	RLRX-DIFF	Differential return loss	10	–	–	dB
Common-mode return loss	RLRX-CM	Common-mode return loss	6	–	–	dB
Unexpected electrical idle enter detect threshold integration time	TRX-IDEL-DET-DIFF-ENTERTIME	An unexpected electrical idle must be recognized no longer than this time to signal an unexpected idle condition.	–	–	10	ms
Signal detect threshold	VRX-IDLE-DET-DIFFp-p	Electrical idle detect threshold	65	–	175	mV
Transmitter						
Output voltage	VTX-DIFFp-p	Differential p-p, programmable in 16 steps	0.8	–	1200	mV
Output voltage rise time	VTX-RISE	20% to 80%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI
Output voltage fall time	VTX-FALL	80% to 20%	0.125 (2.5 GT/s) 0.15 (5 GT/s)	–	–	UI

Table 16: PCI Express Parameters (Cont.)

Parameter	*Symbol*	*Comments*	*Min.*	*Typ.*	*Max.*	*Units*
RX detection voltage swing	VTX-RCV-DETECT	The amount of voltage change allowed during receiver detection.	–	–	600	mV
TX AC peak common-mode voltage (5 GT/s)	VTX-CM-AC-PP	TX AC common mode voltage (5 GT/s)	–	–	100	mV
TX AC peak common-mode voltage (2.5 GT/s)	VTX-CM-AC-P	TX AC common mode voltage (2.5 GT/s)	–	–	20	mV
Absolute delta of DC common-model voltage during L0 and electrical idle	VTX-CM-DC-ACTIVE-IDLE-DELTA	Absolute delta of DC common-model voltage during L0 and electrical idle.	0	–	100	mV
Absolute delta of DC common-model voltage between D+ and D–	VTX-CM-DC-LINE-DELTA	DC offset between D+ and D–	0	–	25	mV
Electrical idle differential peak output voltage	VTX-IDLE-DIFF-AC-p	Peak-to-peak voltage	0	–	20	mV
TX short circuit current	ITX-SHORT	Current limit when TX output is shorted to ground.	–	–	90	mA
DC differential TX termination	ZTX-DIFF-DC	Low impedance defined during signaling (parameter is captured for 5.0 GHz by RLTX-DIFF)	80	–	120	Ω
Differential return loss	RLTX-DIFF	Differential return loss	10 (min.) for 0.05: 1.25 GHz 8 (min.) for 1.25: 2.5 GHz	–	–	dB
Common-mode return loss	RLTX-CM	Common-mode return loss	6	–	–	dB
TX eye width	TTX-EYE	Minimum TX eye width	0.75	–	–	UI
Lane-to-Lane Output Skew	LTX-SKEW	Between any two lanes within a single transmitter	500 + 2 UI (max) at 2.5 GT/s			ps
			500 + 4 UI (max) at 5.0 GT/s			ps

Section 8: Thermal information

Table 17: JEDEC Thermal Characteristics, 13 mm × 13 mm Package [a]

Power Dissipation (W)	3.40				
Ambient Air Temperature (°C)	70				
θ_{JB} (°C/W)	1.03				
θ_{JC} (°C/W)	18.00				
Airflow	0 fpm, 0 mps	100 fpm, 0.508 mps	200 fpm, 1.016 mps	400 fpm, 2.032 mps	600 fpm, 3.048 mps
T_J (°C)	tbd	tbd	tbd	tbd	tbd
θ_{JA} (°C/W)	tbd	tbd	tbd	tbd	tbd
Ψ_{JT} (°C/W)	tbd	tbd	tbd	tbd	tbd

a. No heat sink, TA = 70°C. This is an estimate based on a 4-layer 2s2p PCB and P = (TBD) W.

Note:

- Ambient air temperature: TA = 70°C.
- The BCM43684 is designed and rated for operation at a maximum junction temperature not to exceed 125°C.
- For heatsink attachment, optimized force should be used:
  a. Maximum allowed force during heatsink attachment at room temperature: 24 lb/11 kgf for maximum of 30 seconds.
  b. Maximum allowed sustained force during device lifespan: 12.5 lb/5.7 kgf.

Junction Temperature Estimation and PSI$_{JT}$ Versus Theta$_{JC}$

Package thermal characterization parameter Psi-J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is as follows:

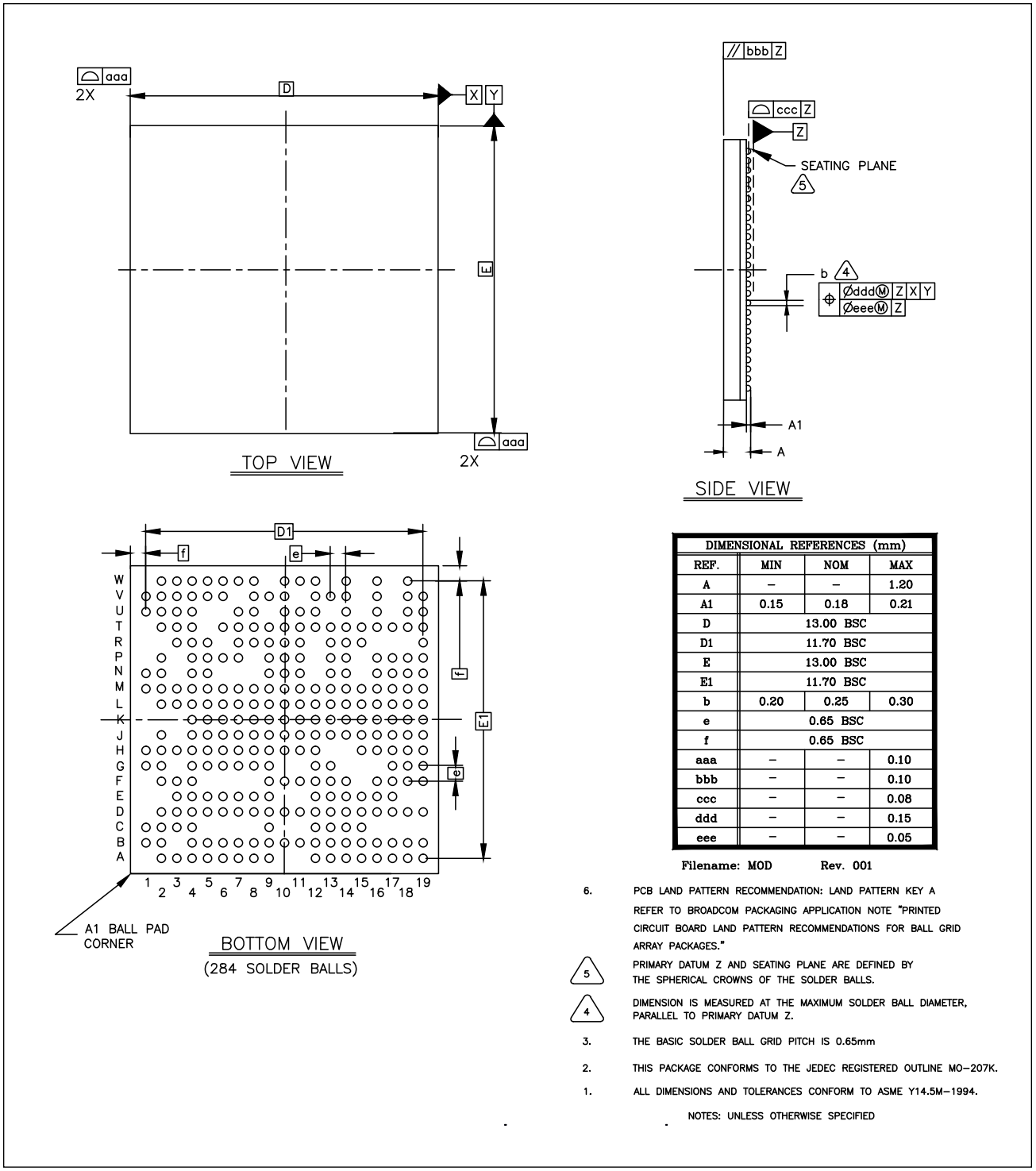
$$T_J = T_T + P \times \Psi_{JT}$$

Where:

- T_J = junction temperature at steady-state condition, °C
- T_T = package case top center temperature at steady-state condition, °C
- P = device power dissipation, Watts
- Ψ_{JT} = package thermal characteristics (no airflow), °C/W

Section 9: Package Information

Figure 12: 284-Pin (13 mm × 13 mm) Mechanical Drawing



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.20
A1	0.15	0.18	0.21
D		13.00 BSC	
D1		11.70 BSC	
E		13.00 BSC	
E1		11.70 BSC	
b	0.20	0.25	0.30
e		0.65 BSC	
f		0.65 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.05

Filename: MOD Rev. 001

6. PCB LAND PATTERN RECOMMENDATION: LAND PATTERN KEY A REFER TO BROADCOM PACKAGING APPLICATION NOTE "PRINTED CIRCUIT BOARD LAND PATTERN RECOMMENDATIONS FOR BALL GRID ARRAY PACKAGES."

5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.65mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–207K.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Section 10: Ordering Information

Table 18: Ordering information

Part Number	*Package*	*Ambient Temperature*
BCM43684A0KFRBG	13 mm × 13 mm, 284-ball RFCBGA (RoHs compliant)	0°C to 70°C

Revision History

Revision	*Date*	*Change Description*
43684-DS100-R	March 10, 2017	Initial release

Web: www.broadcom.com
Corporate Headquarters: San Jose, CA

43684-DS100-R March 10, 2017